COE 571
Digital System Testing
An Introduction

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Outline

- Welcome to COE 571
- VLSI Realization Process
- Definition of Testing
- Reasons for Testing
- Chip Manufacturing Process
- Manufacturing Cost
- Main Difficulties in Testing
- Defects & Faults
- Fault Models
- Automatic Test Pattern Generation

Welcome to COE 571

- **Instructor:** **Dr. Aiman H. El-Maleh**
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Grading Policy

- **Assignments** **15%**
- **Exam I** **15% (S., March 29, 7:00 PM)**
- **Exam II** **20% (S., May 17, 7:00 PM)**
- **Paper Presentations** **10%**
- **Project** **20%**
- **Final** **20%**
  - Attendance will be taken regularly.
  - Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
  - Late assignments will be accepted (upto 3 days) but you will be penalized 10% per each late day.
  - A student caught cheating in any of the assignments will get 0 out of 15%.
  - No makeup will be made for missing Quizzes or Exams.

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Course Topics

- Introduction: The testing problem, costs of testing, test types and schemes.
- Fault modeling: Fault detection and redundancy, fault equivalence, dominance, checkpoints and collapsing. Fault diagnosis. Stuck-at faults, bridging faults, transistor faults, delay faults, etc.
- Fault simulation: serial, parallel, deductive, and concurrent fault simulation. Parallel pattern single fault propagation, critical path tracing and fault sampling.
- Test generation for Combinational circuits: Boolean difference, path sensitization, D-algorithm, PODEM, and FAN. Random test generation, Combined random/deterministic test generation. Test compaction. Cost functions and testability measures.

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Course Topics

- **Test generation for sequential circuits**: Time-frame expansion, extended D-algorithm, BACK algorithm, simulation-based approaches, and complexity of sequential ATPG.
- **Test generation for CMOS circuits**: Test generation for transistor stuck-open and stuck short faults. Test generation based on gate-level models, robust and non-robust test generation.
- **Delay-fault testing**: Gate and path delay fault models, robust, validatable nonrobust and nonrobust test vectors, path delay fault simulation and test generation.

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Course Topics

- **Design for testability: Ad-hoc methods, types of scan cells, LSSD, full scan design, partial scan design, and boundary scan design. Partial scan selection techniques.**
- **Built-in self test: Theory and operation of LFSR, MISR, random and weighted random pattern testability, BIST pattern generator and response analyzer, scan-based BIST architecture, and test point insertion for improving random testability.**

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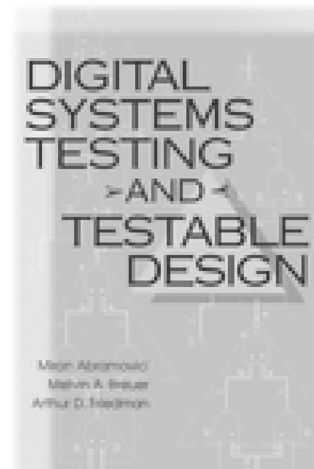
Textbook

- **Digital Systems Testing and Testable Design**

  Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman
- **ISBN: 978-0-7803-1062-9**
- **September 1994, Wiley-IEEE Press**



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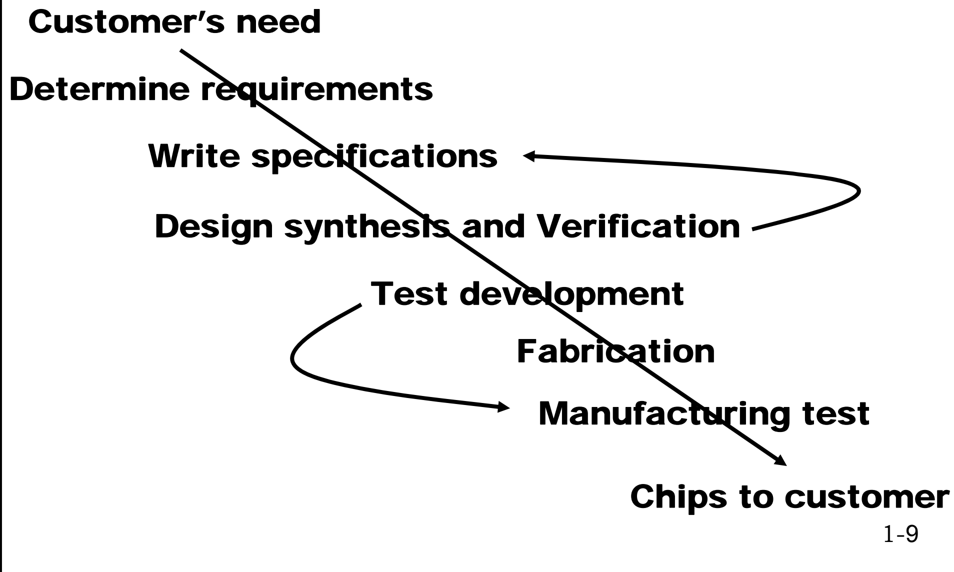
VLSI Realization Process



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Definitions

- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

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Verification vs. Test

Verification

- **Verifies correctness of design.**
- **Performed by simulation, hardware emulation, or formal methods.**
- **Performed once prior to manufacturing.**
- **Responsible for quality of design.**

Test

- **Verifies correctness of manufactured hardware.**
- **Two-part process:**
  - 1. Test generation: software process executed once during design
  - 2. Test application: electrical tests applied to hardware
- **Test application performed on every manufactured device.**
- **Responsible for quality of devices.**

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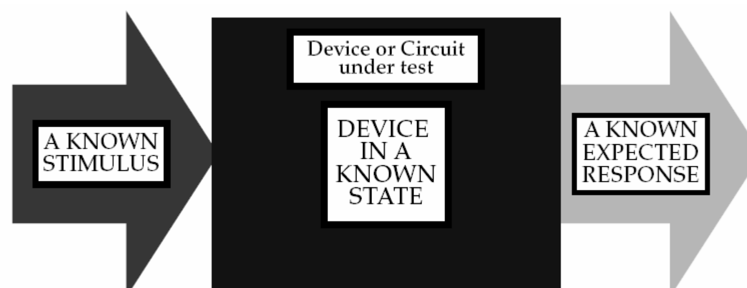
Definition of Testing

- **A *known input stimulus* is applied to a unit in a *known state*, and a *known response* can be evaluated.**



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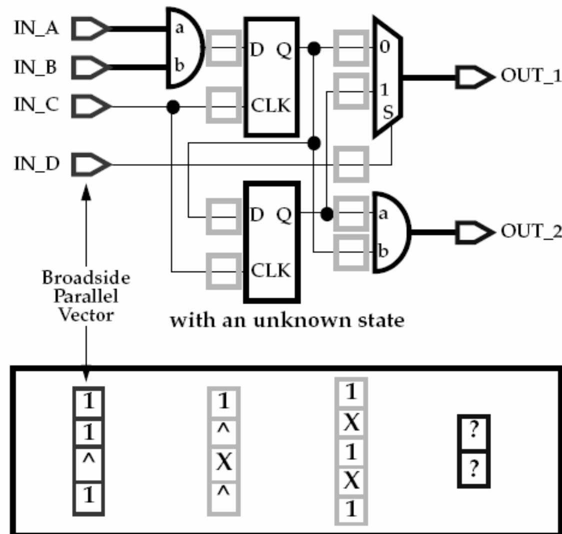
Example



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Reasons for Testing

- **Detection: Determination whether or not the *device under test* (DUT) has some fault.**
  - Measurement of defects and quality level
  - Reliability requirement
- **Diagnosis: Identification of a specific fault that is present on DUT.**
- **Device characterization: Determination and correction of errors in design and/or test procedure.**
- **Failure mode analysis (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.**

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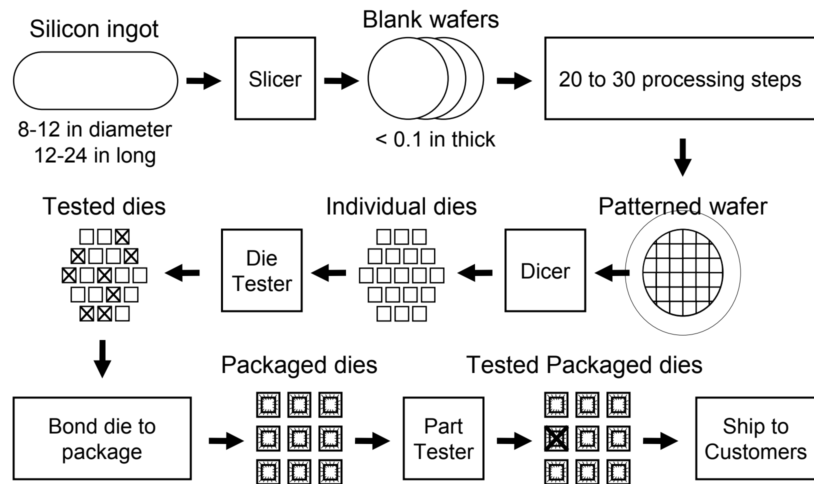
Chip Manufacturing Process



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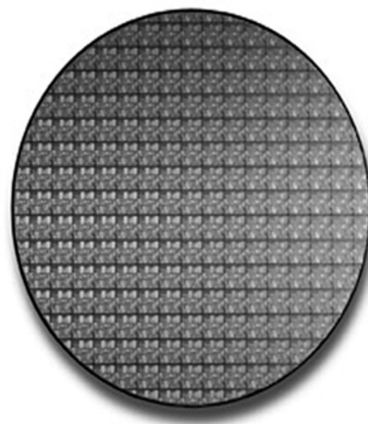
Wafer of Pentium 4 Processors

- **8 inches (20 cm) in diameter**
- **Die area is 250 mm^2**
  - About 16 mm per side
- **55 million transistors per die**
  - 0.18 μm technology
  - Size of smallest transistor
  - Improved technology uses
    - 0.13 μm and 0.09 μm
- **Dies per wafer = 169**
  - When yield = 100%
  - Number is reduced after testing
  - Rounded dies at boundary are useless



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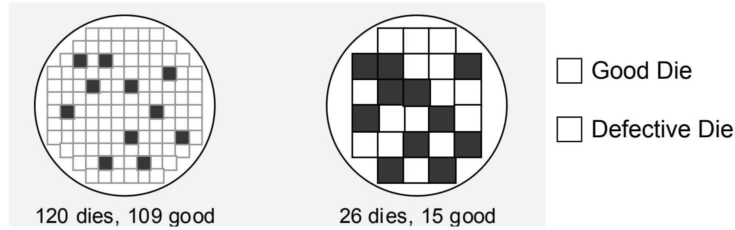
Effect of Die Size on Yield



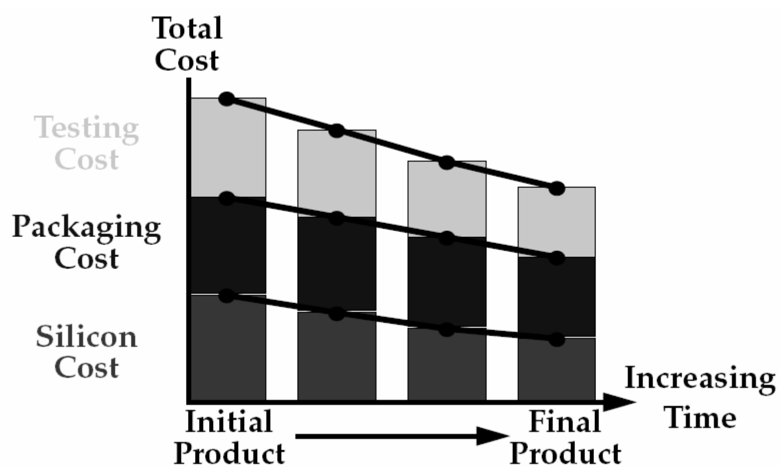
Dramatic decrease in yield with larger dies

Yield = (Number of Good Dies) / (Total Number of Dies)

$$\text{Yield} = \frac{1}{(1 + (\text{Defect per area} \times \text{Die area} / 2))^2}$$

Die Cost = (Wafer Cost) / (Dies per Wafer × Yield)

Product Manufacturing Cost



Product Manufacturing Cost

- **Reduction of silicon cost**
  - increasing volume and yield
  - die size reduction (process shrinks or more efficient layout)
- **Reduction of packaging cost**
  - increasing volume
  - shifting to lower cost packages if possible (e.g., from ceramic to plastic)
  - reduction in package pin count
- **Reduction in cost of test**
  - reducing vector data size
  - reducing the cost of the tester
  - reducing test time

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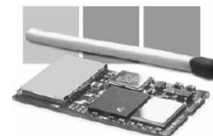
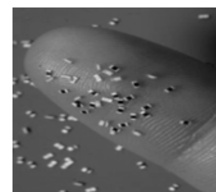
Main Difficulties in Testing

- **Miniaturization ⇨ Physical access difficult or impossible.**
- **Increasing complexity ⇨ Large amount of test data.**
- **Number of access ports remains constant ⇨ Long test application time.**
- **High speed ⇨ High demand on tester's driver/sensor mechanism and more complicated failure mechanism.**
- **Testing accounts up to 50% of product development efforts.**
- **The key to successful testing lies in the design process.**





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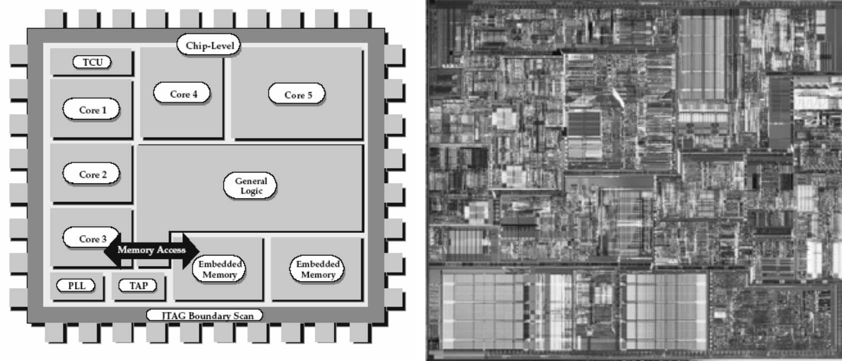
Main Difficulties in Testing



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Costs of Testing

- *Design for testability* (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- **Software processes of test**
  - Test generation and fault simulation
  - Test programming and debugging
- **Manufacturing test**
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost

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Cost of Manufacturing Test

- **0.5-1.0GHz, analog instruments,1,024 digital pins:**
  - ATE purchase price= \$1.2M + 1,024 x \$3,000 = \$4.272M
- **Running cost (five-year linear depreciation)**
  - = Depreciation + Maintenance + Operation
  - = \$0.854M + \$0.085M + \$0.5M
  - = \$1.439M/year
- **Test cost (24 hour ATE operation)**
  - = \$1.439M/(365 x 24 x 3,600)
  - = 4.5 cents/second

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Automatic Test Equipment Components

- **Powerful computer**
- **Powerful 32-bit Digital Signal Processor (DSP) for analog testing**
- **Test Program (written in high-level language) running on the computer**
- **Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)**
- **Probe Card or Membrane Probe (contains electronics to measure signals on chip pin or pad)**

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ADVANTEST Model T6682 ATE

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LTX FUSION HF ATE

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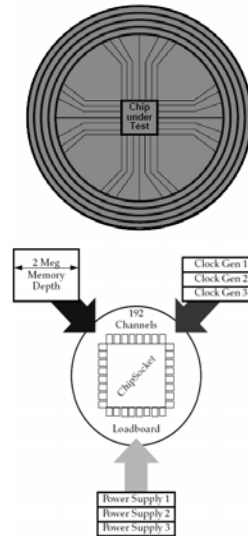
Manufacturing Test Board

- The chip will be accessed by the tester at its pins only
- A custom (load) board will be made for this purpose
- Each pin has a limited number of bits available (e.g., 2 MB)
- Test program (set of vectors and tester control) applied at tester speed (may be less than actual chip speed)
- Primary goal of manufacturing test is structural verification



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Design For Testability

- To take into account the testing aspects during the design process so that more testable designs will be generated.
- Advantages of DFT
  - **Reduce test efforts.**
    - **Eases generation of test vectors**
    - **Eases diagnosis & debugging**
  - **Reduce cost for test equipments (ATE).**
  - **Shorten turnaround time.**
  - **Increase product quality.**
- Disadvantages of DFT
  - **Adds complexity to design methodology**
  - **Impacts design area, power, speed and package pins**

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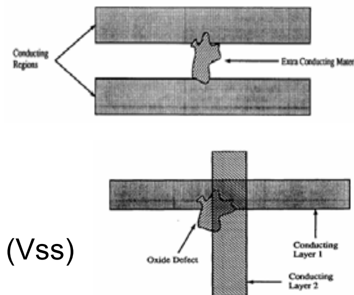
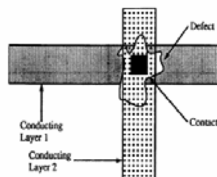
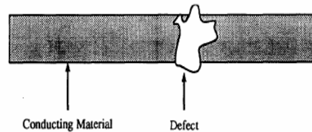
Defects

- **Defects: physical problems that occur in silicon**
- **Common Silicon CMOS defects:**
  - Gate-oxide shorts
  - Insufficient doping
  - Process or mask errors
  - Metal trace opens
  - Metal trace bridges
  - Open and plugged vias
  - Short to power (Vdd) or Ground (Vss)







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Defects

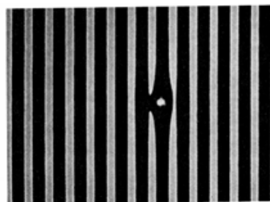

Figure 1: Example of a break in a metal line.

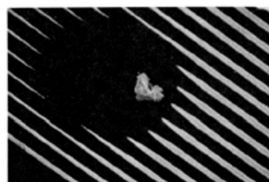

Figure 2: Example of a break of 7 metal lines caused by the interaction between a contaminating particle and the photoresist.

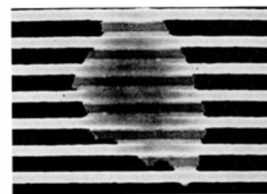

Figure 3: Example of a short of 7 metal lines caused by unexposed photo resist.

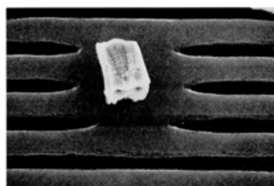

Figure 4: Short of 4 metal lines caused by a solid state particle deposited on the metal layer before metal lithography.

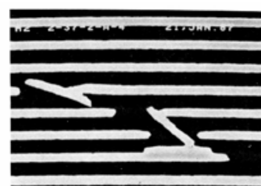

Figure 5: Shorts and breaks of metal lines caused by a scratch in the photoresist.

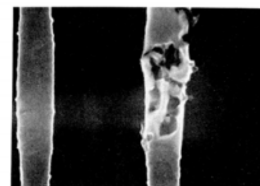

Figure 6: Example of metal line corrosion that eventually may result in breaks.

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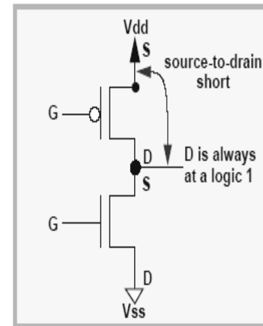
Faults

- **Fault is a model of failure mode of defect that relates defect to circuit behavior.**
- **Example**
  - Gate-Oxide short shorts transistor's source to drain (S2D)
  - Modeled by connecting gate to 0 or 1
  - Transistor Stuck-on or Stuck-off
- **Behavior resulting from these models may be a high current, a high impedance state or intermittent behavior.**



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Common Fault Models

- Single stuck-at faults
- Multiple stuck-at faults
- Transistor open and short faults
- Bridging faults
- Delay faults (transition, path)
- Memory faults
- PLA faults (stuck-at, cross-point, bridging)
- Functional faults (processors)
- Analog faults

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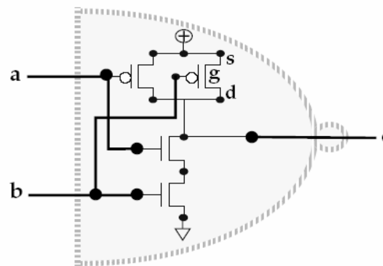
Single Stuck-at Fault Model

- Failures represented as an individual wire shorted to Vdd (stuck-at-1) or Vss (stuck-at-0).
- Covers many of physical defects.
- Number of faults small.
- Independent of technology.
- Can be used to model other type of faults.



stuck faults	
a@ 0	a@ 1
b@ 0	b@ 1
c@ 0	c@ 1
6 gate faults	

Truth Table with fail modes					
nand		ab	a	b	c
ab	c	0	1	1	0
00	1	1	1	1	0
01	1	1	0	1	0
10	1	1	1	0	0
11	0	1	0	0	0

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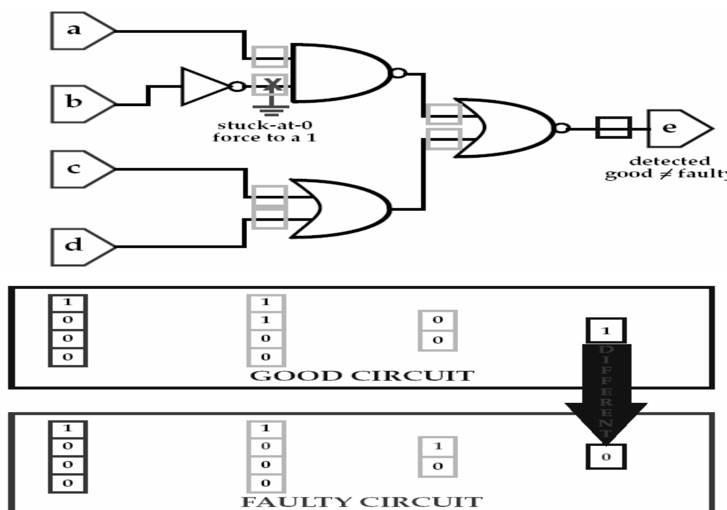
Example



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Multiple Stuck-at Faults

- **A multiple stuck-at fault means that any set of lines is stuck-at some combination of (0,1) values.**
- **The total number of multiple stuck-at faults in a circuit with k single fault sites is 3^k-1.**
- **A single fault test can fail to detect the target fault if another fault is also present, however, such masking of one fault by another is rare.**
- **Statistically, single fault tests cover a very large number of multiple faults.**

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Transistor (Switch) Faults

- **MOS transistor is considered an ideal switch and two types of faults are modeled:**
  - Stuck-open -- a single transistor is permanently stuck in the open state.
  - Stuck-short -- a single transistor is permanently shorted irrespective of its gate voltage.
- **Detection of a stuck-open fault requires two vectors.**
- **Detection of a stuck-short fault requires the measurement of quiescent current (IDDQ).**

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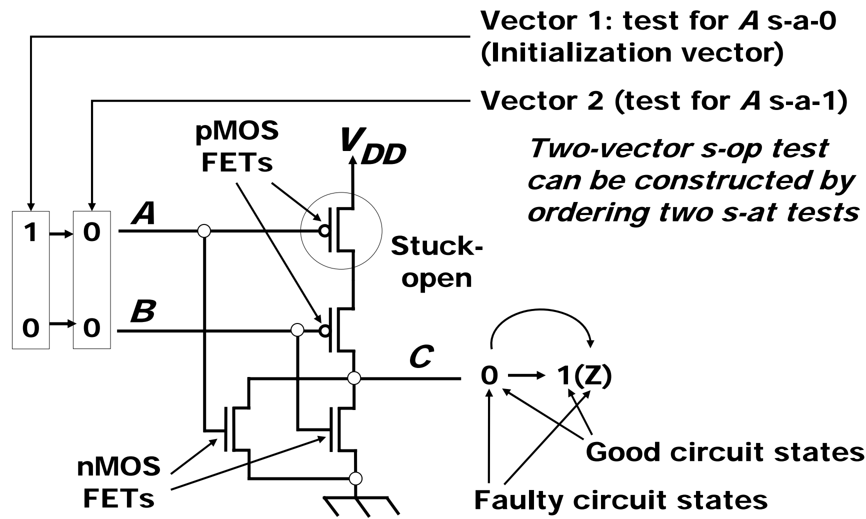
Stuck-Open Example



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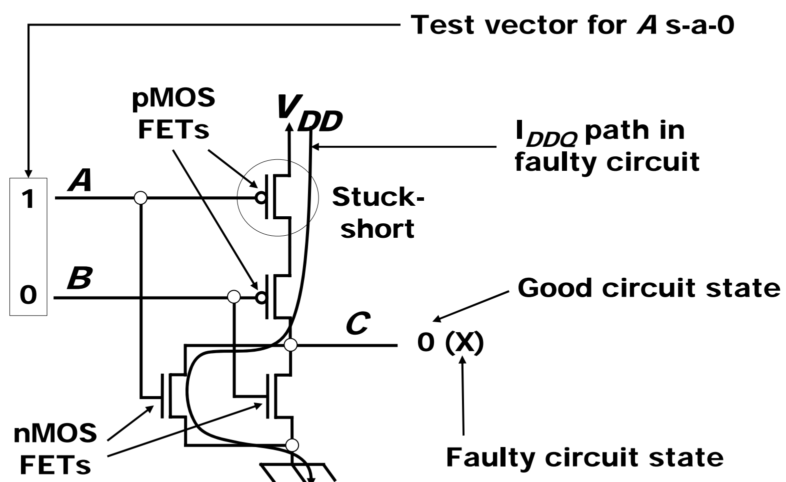
Stuck-Short Example



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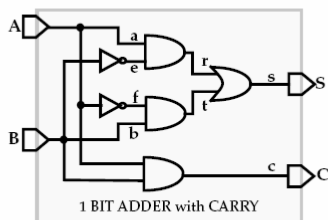
Delay Faults

- **Some defects do not manifest a logical incorrect behavior but appear as an increase in delay**
- **Example**
  - Small metal open on a connection trace
  - Logic value still propagates
  - Propagation of value is slowed down

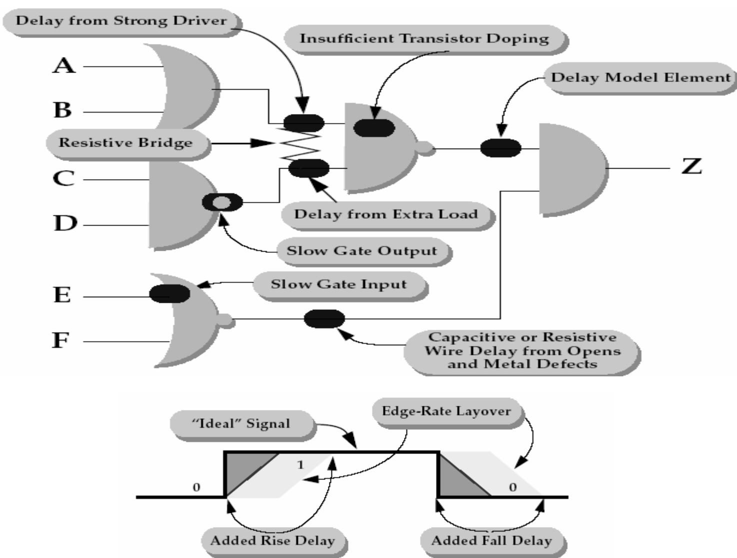


transition delay faults	
a1- 0	a0- 1
b1- 0	b0- 1
c1- 0	c0- 1
6 transitions	

path delay faults	
A2SR	A2SF
A2CR	A2CF
B2SR	B2SF
B2CR	B2CF
path	

R=Slow-to-Rise
F=Slow-to-Fall

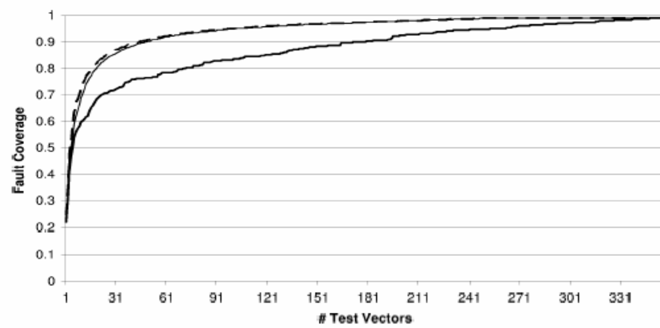
Example



Fault Coverage

- **Used as measure of test quality**

$$Fault\ Coverage = \frac{Detected\ Faults}{Number\ of\ Faults}$$



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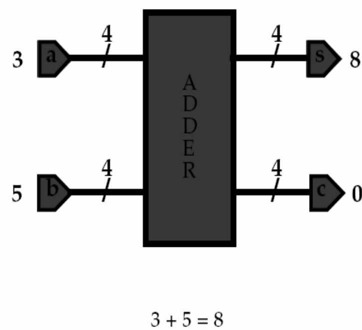
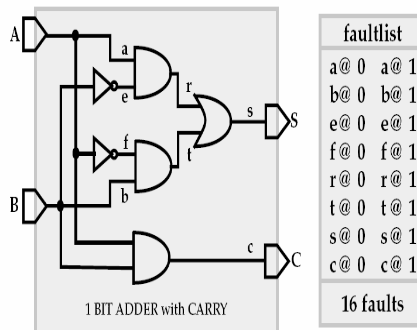
Types of Testing





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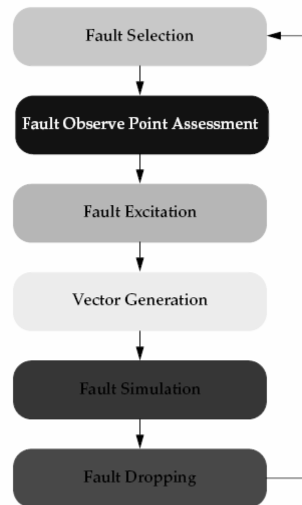
Automatic Test Pattern Generation

- **Eases generation of test vectors.**
- **Reduces cost of test**
  - More efficient test vectors
  - Reduction in cycle time
- **Provides a deterministic quality metric.**



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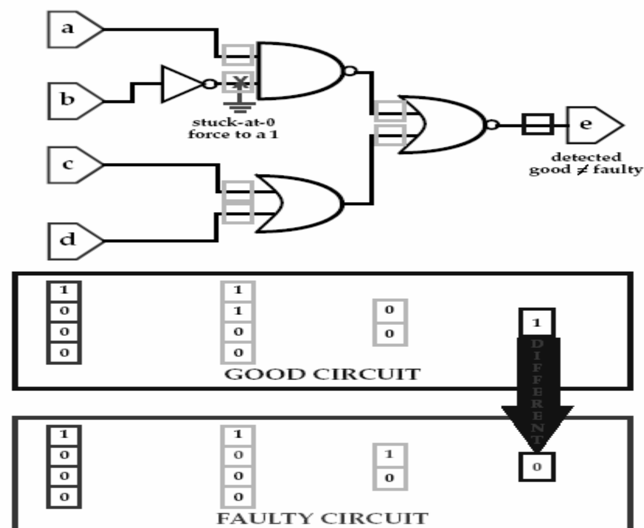
Detectable Fault



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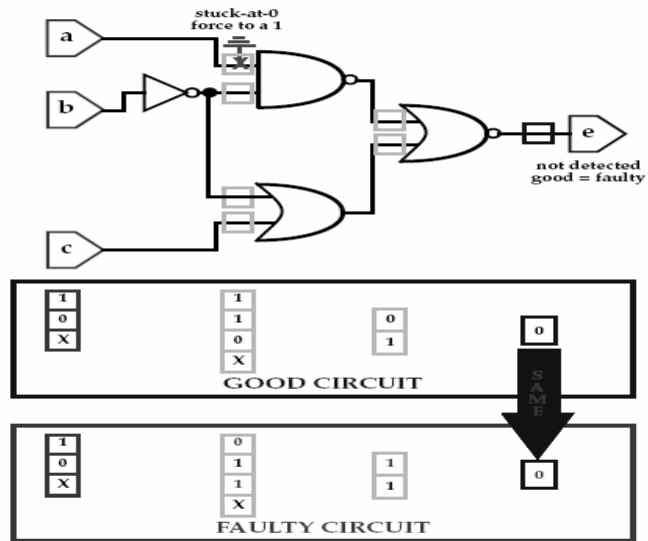
Undetectable Fault



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