COE 545, Term 992

Digital System Testing

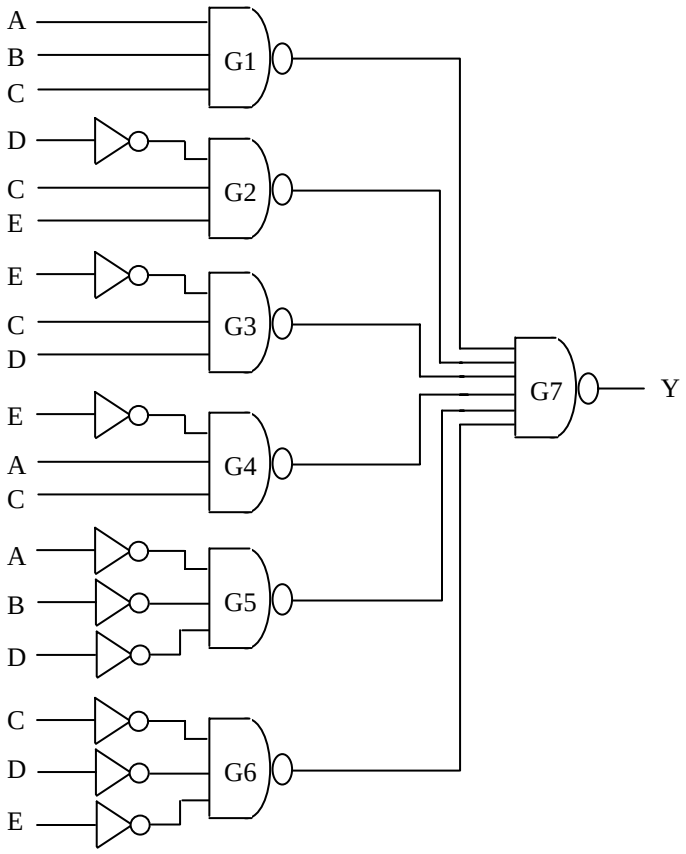
HW#4

Due date: Tuesday, April 25

Q.1. Problem 6.32

Q.2. Problem 6.33

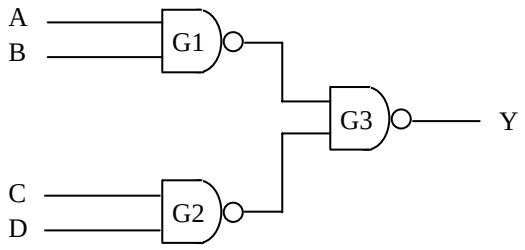
Q.3. Consider the circuit shown below:



(i) Verify using HITEC that all the single stuck-at faults in the circuit are detectable.

(ii) Generate all the tests that detect the TSOP fault in the pMOS transistor of gate G7 driven by the output of gate G4. Determine if any of those tests is a robust test.

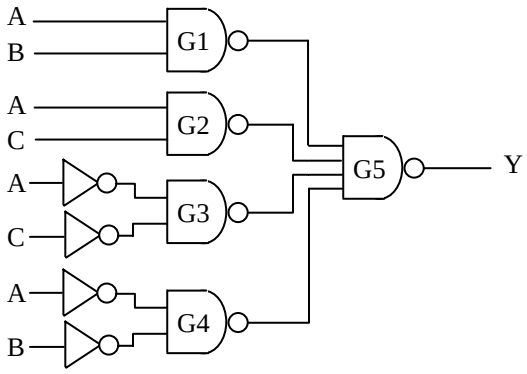
Q.4. Consider the circuit shown below composed of three 2-input static CMOS NAND gates.



(i) Determine the transistor stuck-open faults in the circuit that are robustly testable by the test set {1101, 0101, 1110, 1010, 0111, 0101, 1011, 1010}. Assume that the vectors are applied in the order given. What are your observations?

(ii) Generate a minimal test set that robustly detects all the transistor stuck-open faults in the circuit.

Q.5. Consider the two-level circuit shown below:



(i) Are all the path delay faults in the circuit robustly testable. If not, identify the paths that are not robustly delay fault testable.

(ii) Are all the path delay faults in the circuit validatable non-robust (VNR) testable. If yes, derive a complete VNR test set for all the paths. Otherwise, identify those that are not VNR testable.

(iii) Are all the gate delay faults robustly testable. If yes, derive a complete robust test set for all the gate delay faults. Otherwise, identify those that are not robustly testable.

(iv) Reimplement the function Y such that in the new implementation all the path delay faults are robustly testable.

Q.6. Consider the CMOS circuit shown below. Derive tests for detecting all the detectable transistor stuck-open and transistor stuck-short faults in the circuit using the following methods. Determine the faults that require current monitoring for their detection.

(i) B-Block method

(ii) Second gate-level based method given in class.