COE 545, Term 992

Digital System Testing

HW#3

Due date: Sunday, April 2

Q.1. Problem 6.17

Q.2. Problem 6.22

Q.3. Problem 6.23

Q.4. Problem 6.24

Q.5. Problem 6.26

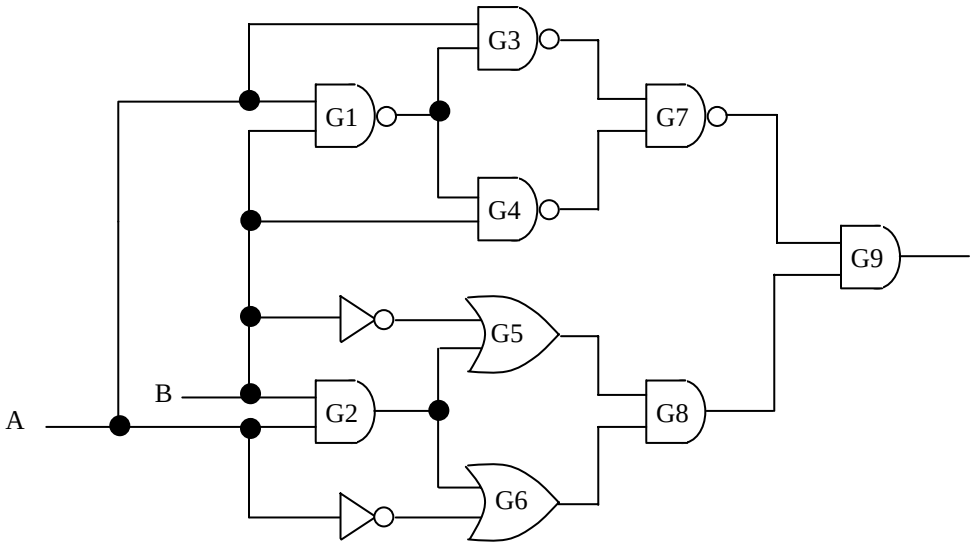
Q.6. Problem 6.28

Q.7. Problem 6.31

Q.8. Consider the circuit shown below. Use both PODEM and FAN algorithms to generate tests for the following faults. Show the steps done by each of the algorithms in detail including the decision tree:

(i) G2 stuck-at-1.

(ii) G9 stuck-at-0.



Q.9. Consider the Combinational circuit c7552.bench with 207 primary inputs and 108 primary outputs. This circuit has a set of 7550 collapsed faults out of which 7417 faults are detectable and the rest are redundant.

(i) Generate a random set of test vectors for this circuit by applying sets of 10 vectors, in sequence, and plot the fault coverage achieved versus the number of vectors applied. Stop generating a new set of 10 test vectors if no new faults are detected by the last set of 10 test vectors applied. Compact the test generated by eliminating vectors that do not detect any fault and also based on reverse order fault simulation.

(ii) Use HITEC to generate deterministic patterns for this circuit. If the detectable faults are not completely detected after two iterations then stop HITEC. Plot the fault coverage achieved versus the number of test vectors applied, and compare it to the one in (i). Compact the generated test set as in (i). Compare the generated test sets in (i) and (ii) in terms of fault coverage, test set length, CPU time and comment on the results.

(iii) Apply a two-phase approach where random vectors are applied first until improvement in the fault coverage from the last 10 vectors applied is less than 2%. Then, store the vectors randomly generated in c7552.vec. After that modify the TEST.run file generated by the command *do_hitec* to enable HITEC to fault simulate the vectors in c7552.vec before starting the ATPG process. Compare the test set generated using this approach to the ones generated in (i) and (ii) in terms of fault coverage, test set length, and CPU time.

Q.10. Apply the RAPS procedure to generate 4 vectors for the circuit in Figure 6.53. Then, use a random test generator to generate 4 random vectors. Fault simulate the vectors generated by RAPS and those generated randomly and compare the fault coverage achieved.