COE 545, Term 992

Digital System Testing

HW#2

Due date: Tuesday, March 7

Q.1. For the circuit in Figure 5.38, determine the faults detected by the tests {111, 011} for each of the following methods, starting with a collapsed fault set based on fault equivalence. Show the details of each method.

(i) Deductive fault simulation.

(ii) Critical path tracing.

(iii) Concurrent fault simulation.

Q.2. Problem 6.3

Q.3. Problem 6.4.

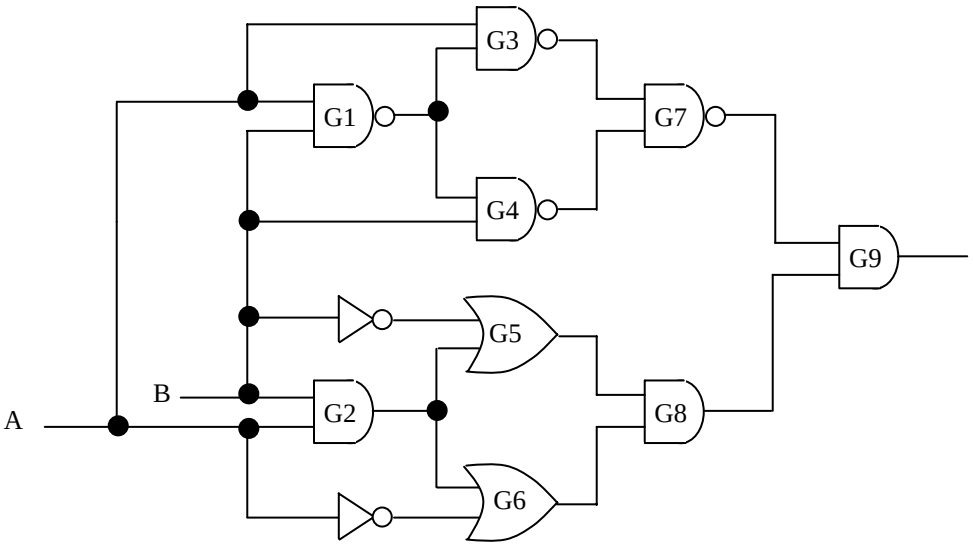
Q.4. Problem 6.5.

Q.5. Problem 6.6.

Q.6. Consider the circuit shown below. Use the D-algorithm to generate tests for the faults shown below. Show the steps done by the algorithm in detail including the decision tree, the D-frontier, and the J-frontier:

(i) G2 stuck-at-1.

(ii) G9 stuck-at-0.



Q.7. Consider the full-scanned version of the circuit s38417 given as s38417f.bench. The number of collapsed faults in this circuit is 31180. The test set s38417f.vec detects 31004 faults, i.e. producing a fault coverage equal to 99.44%.

(i) Perform fault simulation of the test set on a randomly selected sample of *m* faults for each of the following values of *m: 100, 1000, and 5000*. Determine the fault coverage obtained, compare it to the exact fault coverage, and determine the error in each case.

(ii) Reverse the order of the test vectors in s38417f.vec. Then, fault simulate the reversed test set on all the faults and remove the vectors that no longer detect any fault. Repeat this process till the test set can not be further reduced. Comment on why the test set can be reduced by doing this procedure.

Q.8. PROOFS is a fast fault simulator for sequential circuits. Study the algorithm from the paper shown below and briefly describe the main technique of fault simulation employed by the simulator.

> *T.M. Nierman, W.-T. Cheng, and J. H. Patel, ``PROOFS: A fast, memory-efficient sequential circuit fault simulator,`` IEEE Trans. Computer-Aided Design, vol. 11, no. 2, pp. 198-207, February 1992.*