COE 545, Term 992

Digital System Testing

HW# 1

Due date: Sunday, Feb. 6

Q.1. Problem 4.8.

Q.2. Problem 4.10.

Q.3. Problem 4.12.

Q.4. Problem 4.16.

Q.5. Problem 4.17.

Q.6. Given a manufacturing process with a certain yield Y and a test with certain fault coverage. Plot the Defect level (DL) curve as a function of the fault coverage for the cases when the yield Y=0.2, 0.4, 0.6 and 0.8 based on the following:

(i) Formula derived in class.

(ii) The Williams and Brown model: $DL=1-(Y)^{(1-d)}$, where d is the defect coverage of the test. Assume that d is equal to the fault coverage as an approximation. Compare the defect level curves in (i) and (ii).

Q.7. Consider an n-input XOR gate:

(i) Determine the minimum number of SSFs faults that has to be targeted to detect all the SSFs in the gate.

(ii) Determine the minimum number of test vectors required to detect all the SSFs.

Q.8. Let Z(x) be the function of a single-output Combinational circuit N.

(i) Give an example of a single stuck-at fault that changes the function from Z(x) to Z(x)`.

(ii) Show that if N is an irredundant circuit, then none of the SSFs in N can change its function from Z(x) to Z(x)`.

Q.9. Consider the circuit shown in Figure 4.23:

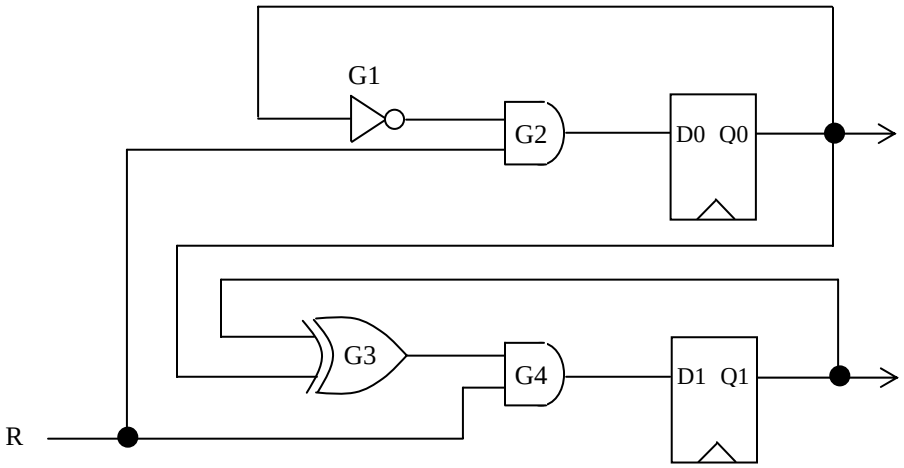
(i) Starting with injecting faults on each line in the circuit, perform fault collapsing using fault equivalence relation.

(ii) Starting with injecting faults on each line in the circuit, perform fault collapsing using fault equivalence and dominance relations.

(iii) Starting with the set of faults based on the checkpoint theorem (Theorem 4.2), perform fault collapsing using the equivalence and dominance relations. Compare the set of collapsed faults to what you obtained in (ii).

(iv) Perform fault collapsing using HITEC. Compare the collapsed fault set to what you obtained in (ii) & (iii).

Q.10. Consider the 2-bit counter shown below, where Q0 and Q1 are primary outputs and R is a primary input:



(i) Derive a test sequence for detecting the fault G3 s-a-0. Verify your result by fault simulation using PROOFS.

(ii) Identify the SSFs in the circuit that prevent initialization. Then, determine whether these faults can be detected or not and under what conditions. Check whether these faults can be detected by HITEC or not and comment on the answer.