COE 545, Term 022

Digital System Testing

HW# 1

Due date: Sunday, March 23

Q.1. Problem 4.8.

Q.2. Problem 4.10.

Q.3. Problem 4.12.

Q.4. Problem 4.16.

Q.5. Given a manufacturing process with a certain yield Y and a test with a certain fault coverage. Plot the Defect level (DL) curve as a function of the fault coverage for the cases when the yield Y=0.1, 0.2, 0.4, 0.6, 0.8, and 0.9 based on the following:

    (i) Formula derived in class.

    (ii) The Williams and Brown model: $DL=1-(Y)^{(1-d)}$, where d is the defect coverage of the test. Assume that d is equal to the fault coverage as an approximation. Compare the defect level curves in (i) and (ii).

Q.6. Consider an n-input Exclusive OR (XOR) gate as a compound gate (i.e. consider the faults only on its inputs and output):

    (i) Determine the number of SSFs after equivalence fault collapsing.

    (ii) Determine the number of SSFs after equivalence and dominance fault collapsing.

    (iii) Determine the minimum number of test vectors required to detect all the SSFs.

Q.7. Consider the circuit shown in Figure 4.6

    (i) Find a complete detection test set that detects all the faults in the circuit. Verify your answer by fault simulating the test set using PROOFS.

    (ii) Find a complete location test set that distinguishes between every pair of distinguishable faults in the circuit. Derive the fault dictionary for the circuit.

Q.8. Consider the circuit shown in Figure 4.23:

    (i) Starting with injecting faults on each line in the circuit, perform fault collapsing using fault equivalence relation.

    (ii) Starting with injecting faults on each line in the circuit, perform fault collapsing using fault equivalence and dominance relations.

    (iii) Starting with the set of faults based on the checkpoint theorem (Theorem 4.2), perform fault collapsing using the equivalence and dominance relations. Compare the set of collapsed faults to what you obtained in (ii).

    (iv) Perform fault collapsing using HITEC. Compare the collapsed fault set to what you obtained in (ii) & (iii).

Q.9. Let $Z(x)$ be the function of a single-output Combinational circuit N.

    (i) Give an example of a single stuck-at fault that changes the function from $Z(x)$ to $Z(x)`$.

    (ii) Show that if N is an irredundant circuit, then none of the SSFs in N can change its function from $Z(x)$ to $Z(x)`$.

Q.10. Consider the sequential circuit shown below, where Q1 is a primary output and R is a primary input:
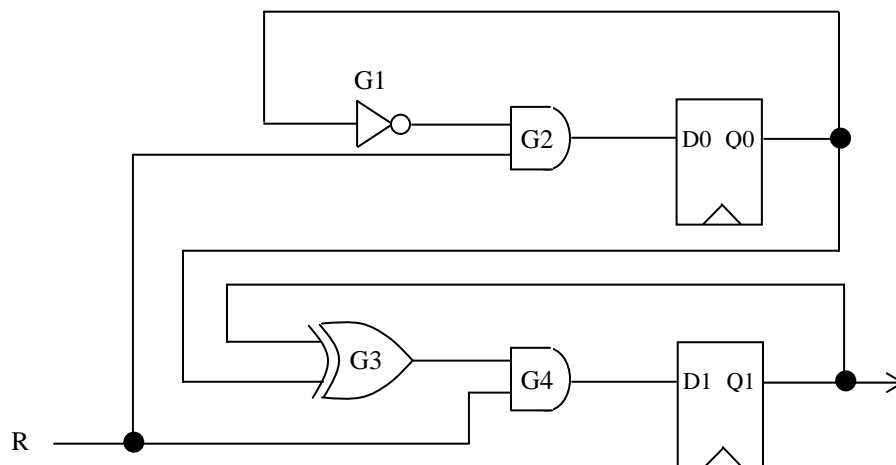
    (i) Show an iterative array model of four time frames for this circuit.

    (ii) Derive a test sequence for detecting the fault G2 s-a-0. Verify your result by fault simulation using PROOFS.

    (iii) Determine whether the fault R s-a-1 is detectable, strongly detectable, partially testable or redundant. Check whether the fault can be detected by HITEC or not and comment on the answer.