COE 545
Digital System Testing
Course Project: Survey
FPGA Testing: List of Papers

You are to survey a set of at least 10 papers in a particular topic in the FPGA testing area. A list of papers covering the different topics is given below. Cover the most recent papers if there are more than 10. You can cover any of the following areas:

1. **Test Methodology**
2. **Diagnosis**
3. **Delay Fault Testing**
4. **Built-In Self Test**
5. **Online Testing**
6. **Fault Modeling, Test Pattern Generation, Fault Grading, Design For Testability**

Test Methodology

Testing interconnects of dynamic reconfigurable FPGAs
Chi-Feng Wu   Cheng-Wen Wu
Dept. of Electr. Eng., Nat. Tsing Hua Univ., Hsinchu;
This paper appears in: Design Automation Conference, 1999. Proceedings of the ASP-DAC '99. Asia and South Pacific
01/18/1999 -01/21/1999, 18-21 Jan 1999
Location: Wanchai ,   Hong Kong
On page(s): 279-282 vol.1
18-21 Jan 1999
References Cited: 10
IEEE Catalog Number: 99EX198
Number of Pages: (xxvi+372+suppl.)
INSPEC Accession Number: 6358303
Abstract:
Field Programmable Gate Arrays (FPGAs) are an increasingly popular choice for fast prototyping and for products whose time to market is relatively short. Testing FPGAs before programming them is thus becoming a major concern to the manufacturers as well as the users. In this paper we propose a universal test for the interconnects of typical dynamic reconfigurable FPGAs. The proposed test configurations and corresponding test patterns for the Xilinx XC6200 FPGAs are shown to cover all interconnect faults. In our test, the total number of test configurations is only 7, which is independent of the FPGA size. The test time for XC6216 is less than 5 ms

Testing the unidimensional interconnect architecture of symmetrical SRAM-based FPGA
Renovell, M.   Faure, P.   Prinetto, P.   Zorian, Y.
LIRMM-UM2, Montpellier;
This paper appears in: Electronic Design, Test and Applications, 2002. Proceedings. The First IEEE International Workshop on

01/29/2002 -01/31/2002, 2002
Location: Christchurch , New Zealand
On page(s): 297-301
2002
References Cited: 15
Number of Pages: xvii+517
INSPEC Accession Number: 7327817
Abstract:
This paper proposes a new and original solution to test the unidimensional interconnect architecture of a RAM based FPGA by exploring the specific properties of these blocks. The method to find a reduced set of configurations is proposed and the sequence of test vectors required for each configuration is given

FPGA test and coverage
Toutounchi, S. Lai, A.
This paper appears in: Test Conference, 2002. Proceedings. International
On page(s): 599- 607
2002
ISSN: 1089-3539
Number of Pages: xvi+1250
INSPEC Accession Number: 7528829
Abstract:
This paper presents an FPGA test and coverage methodology. BIST and "shift register" styles of test are discussed. Gate level fault grading results are then presented. Use of an "iterative logic unit" and its impact on test and fault grading is discussed.

Universal test complexity of field-programmable gate arrays
Inoue, T. Fujiwara, H. Michinishi, H. Yokohira, T. Okamoto, T.
Graduate Sch. of Inf. Sci., Nara Inst. of Sci. & Technol.;
This paper appears in: Test Symposium, 1995., Proceedings of the Fourth Asian
11/23/1995 -11/24/1995, 23-24 Nov 1995
Location: Bangalore , India
On page(s): 259-265
23-24 Nov 1995
References Cited: 8
INSPEC Accession Number: 5285768
Abstract:
A field-programmable gate array (FPGA) can implement arbitrary logic circuits in the field. In this paper we consider universal test such that when applied to an unprogrammed FPGA, it ensures that all the corresponding programmed logic circuits on the FPGA are fault-free. We focus on testing for look-up tables in FPGAs, and present two types of programming schemes; sequential loading and random access loading. Then we show test procedures for the FPGAs with these programming schemes and their test complexities. In order to make the test complexity for FPGAs independent of the array size of the FPGAs, we propose a programming scheme called block-sliced loading, which makes FPGAs C-testable

Testing configurable LUT-based FPGA's
Wei Kang Huang Meyer, F.J. Xiao-Tao Chen Lombardi, F.
Dept. of Electron. Eng., Fudan Univ., Shanghai ;
This paper appears in: Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
On page(s): 276-283
Volume: 6, Issue: 2, Jun 1998
ISSN: 1063-8210
References Cited: 14

CODEN: IEVSE9
INSPEC Accession Number: 5944454
Abstract:
We present a new technique for testing field programmable gate arrays (FPGA's) based on look-up tables (LUT's). We consider a generalized structure for the basic FPGA logic element (cell); it includes devices such as LUT's, sequential elements (flip-flops), multiplexers and control circuitry. We use a hybrid fault model for these devices. The model is based on a physical as well as a behavioral characterization. This permits detection of all single faults (either stuck-at or functional) and some multiple faults using repeated FPGA reprogramming. We show that different arrangements of disjoint one-dimensional (I-D) cell arrays with cascaded horizontal connections and common vertical input lines provide a good logic testing regimen. The testing time is independent of the number of cells in the array (C-testability), We define new conditions for C-testability of programmable/reconfigurable arrays. These conditions do not suffer from limited I/O pins. Cell configuration affects the controllability/observability of the iterative array. We apply the approach to various Xilinx FPGA families and compare it to prior work

Novel technique for testing FPGAs
Metra, C.   Mojoli, G.   Pastore, S.   Salvi, D.   Sechi, G.
Dipt. di Elettronica Inf. e Sistemistica, Bologna Univ.;
This paper appears in: Design, Automation and Test in Europe, 1998., Proceedings
02/23/1998 -02/26/1998, 23-26 Feb 1998
Location: Paris ,   France
On page(s): 89-94
23-26 Feb 1998
References Cited: 18
Number of Pages: xxxiv+993
INSPEC Accession Number: 5912344
Abstract:
This paper presents a novel technique for testing Field Programmable Gate Arrays (FPGAs), suitable for use in the case of frequent FPGA reuse and rapid dynamic modifiability of the implemented function

Array-based testing of FPGAs: architecture and complexity
Huang, W.K.   Meyer, F.J.   Lombardi, F.
Dept. of Electron. Eng., Fudan Univ., Shanghai ;
This paper appears in: Innovative Systems in Silicon, 1996. Proceedings., Eighth Annual IEEE International Conference on
10/09/1996 -10/11/1996, 9-11 Oct 1996
Location: Austin, TX ,   USA
On page(s): 249-258
9-11 Oct 1996
References Cited: 4
Number of Pages: vii+391
INSPEC Accession Number: 5495902
Abstract:
This paper analyzes the architectural and complexity features of the array-based testing technique for field programmable gate arrays (FPGAs). The analysis is pursued using a hybrid (functional/stuck-at) single fault model by considering both the architecture of the configurable logic block (CLB) as well as the whole FPGA. Its evaluation using three commercially available FPGA families by Xilinx is presented in detail; emphasis is given to the different array configurations which permit the observability/controllability requirements of the testing process to satisfy the input/output restrictions (given by the I/O pins) of the FPGA, while still reducing the number of required programming phases

A structural test methodology for SRAM-based FPGAs

Renovell, M.
LIRMM, Montpellier, France;

This paper appears in: Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium on
On page(s): 385-
2002
ISSN:
Number of Pages: xiv+390
INSPEC Accession Number: 7516591

Abstract:
Summary form only given. This presentation focuses on SRAM-based FPGAs. Their simplicity and flexibility for user changes in the field make this type of FPGA a very popular choice among designers. The architecture and design of these devices have been widely investigated during the last decade, but their test challenges have received less attention. Only recently researchers have addressed the problem of testing FPGAs after manufacturing, in other words, before user programming of specific functions.
Testing before programming presents a wide spectrum of problems, for which a number of researchers have proposed innovative solutions. Testing an FPGA chip poses a challenging problem for test engineers. It requires implementing various configurations (programmings) of the FPGA. But changing configurations incurs reprogramming costs. So the fundamental question for FPGA testing is how can we determine the minimum number of test configurations and corresponding vector test sequences that will cover all the faults of a given FPGA's fault model? Solutions are presented in the presentation for various architectural elements of SRAM-based FPGAs.

A novel approach to testing LUT-based FPGAs

Shyue-Kung Lu   Cheng-Wen Wu
Dept. of Electron. Eng., Fu Jen Catholic Univ., Taipei;

This paper appears in: Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on
05/30/1999 -06/02/1999, Jul 1999
Location: Orlando, FL ,   USA
On page(s): 173-177 vol.1
Volume: 1,   Jul 1999
References Cited: 11
IEEE Catalog Number: 99CH36349
Number of Pages: 6 vol. (liv+565+717+568+604+647+527)
INSPEC Accession Number: 6382172

Abstract:
A novel approach to testing look-up table (LUT) based field programmable gate arrays (FPGAs) is proposed in this paper. A general structure for the basic configurable logic array blocks (CLBs) is assumed. We group k CLBs in the column into a cell, where k denotes the number of inputs of a LUT. The whole chip is partitioned into disjoint one-dimensional arrays of cells. We assume that in each linear array, there is at most one faulty cell, and a faulty cell may contain multiple faulty CLBs. For the LUT, a fault may occur at the memory matrix, decoder, input or output lines. The stuck-on and stuck-off fault models are adopted for multiplexers. Our idea is to configure the cells to make each cell function bijective. In order to detect all faults defined, k+1 configurations are required. For each configuration, a minimal complete input sequence is applied to the leftmost cells of each linear array and the outputs of the rightmost cells can be observed. The input patterns can be easily generated with a k-bit counter and the resulting fault coverage is 100%

On the complexity of sequential testing in configurable FPGAs

Feng, W.   Huang, W.K.   Meyer, F.J.   Lombardi, F.
Dept. of Comput. Sci., Texas A&M Univ., College Station, TX;

This paper appears in: Defect and Fault Tolerance in VLSI Systems, 1998. Proceedings., 1998 IEEE International Symposium on
11/02/1998 -11/04/1998, 2-4 Nov 1998
Location: Austin, TX , USA
On page(s): 164-172
2-4 Nov 1998
References Cited: 8
IEEE Catalog Number: 98EX223
Number of Pages: xi+355
INSPEC Accession Number: 6214854
Abstract:
This paper addresses the issues pertaining to testing field programmable gate arrays (FPGAs) using an array-based technique. In particular, the issues of testing configurable devices (such as multiplexers and flip-flops) in the sequential array process (as the most significant factor for assessing complexity) and the arrangement for pipelining test vectors are treated in detail. Initially testing procedures for a configurable flip-flop and a programmable multiplexer are presented. At system-level, two new pipeline arrangements referred to as the quasi-pipeline and normal pipeline structures are proposed for reducing the number of programming phases. The application of the proposed approaches to the XC4000 FPGA family is also presented

A XOR-tree based technique for constant testability of configurable FPGAs
Huang, W.K.; Zhang, M.Y.; Meyer, F.J.; Lombardi, F.;
Test Symposium, 1997. (ATS '97) Proceedings., Sixth Asian , 17-19 Nov 1997
Page(s): 248 -253
Abstract:
Not available.

SRAM-based FPGAs: a structural test approach
Renovell, M.
Lab. d Inf. Robotique et Microelectron. de Montpellier;
This paper appears in: Integrated Circuit Design, 1998. Proceedings. XI Brazilian Symposium on
09/30/1998 -10/03/1998, 30 Sep-3 Oct 1998
Location: Rio de Janeiro , Brazil
On page(s): 67-72
30 Sep-3 Oct 1998
References Cited: 30
IEEE Catalog Number: 98EX216
Number of Pages: xv+250
INSPEC Accession Number: 6147318
Abstract:
This paper presents a structural approach for testing SRAM-based FPGAs taking into account the configurability of such flexible devices. The SRAM-based FPGA architecture is first discussed identifying the specific FPGA test problems as well as the FPGA test properties. The FPGA architecture is then conceptually divided into different architectural elements such as the logic cells, the interconnect cells and the RAM cells. For each architectural element appropriated fault models are proposed, and test configurations and test vectors are derived targeting the fault models under consideration. Taking into account the extremely long time required for SRAM-based FPGA re-configuration, the main objective of the proposed structural approach is the minimization of the number of test configurations

RAM-Based FPGA's: A Test Approach for the Configurable Logic

M. Renovell, J. M. Portal, LIRMM-UM2
J. Figueras, UPC Diagonal
Y. Zorian , Logic Vision Inc.

Design Automation and Test in Europe (DATE '98)
February 23 - 26, 1998
Paris, France

This paper proposes a methodology for testing the configurable logic of RAM-based FPGAs taking into account the configurability of such flexible devices. The methodology is illustrated using the XILINX 4000 family. On this example of FPGA, we obtain only 8 basic Test Configurations to fully test the whole matrix of CLBs. In the proposed Test Configurations, all the CLBs have exactly the same configuration forming a set of one-dimensional iterative arrays. The iterative arrays present a C-testability property in such a way that the number of Test Configurations 8 is fixed and independent of the FPGA size.

Application-dependent testing of FPGAs for bridging faults

Author
Mehdi Baradaran Tahoori Stanford University, Stanford, CA

Sponsors
ACM : Association for Computing Machinery
SIGADA : ACM Special Interest Group on Ada Programming Language

Publisher
ACM Press New York, NY, USA

Pages: 248 - 248 Series-Proceeding-Section-Article
Year of Publication: 2003
ISBN:1-58113-651-X

ABSTRACT

A new technique is presented for testing for bridging faults in the interconnects of an arbitrary design implemented in an FPGA. The configuration of the routing resources used in the original design remains unchanged in the test configurations. Only the logic blocks used in the design are reprogrammed in order to implement single-term functions, logic functions with only one minterm or one maxterm. As shown by formal proofs, all activated faults are detected when single-term functions and appropriate test vectors are used. As presented in the paper, only two test configurations are necessary to detect all bridging faults, achieving 100% fault coverage. An algorithm is presented for test configuration and test vector generation for the entire FPGA. Also, test vector and configuration generation problem is systematically converted to a satisfiability problem, and state of the art SAT-solvers are exploited for automatic test vector and configuration generation.

FPGAs in digital testing

Garcia Jimenez, A. Garcia Munoz, M.
Indra Sistemas;
This paper appears in: **AUTOTESTCON Proceedings, 2002. IEEE**

On page(s): 11- 29
2002
ISSN: 1080-7725

Abstract:
Not Available

A test methodology for interconnect structures of LUT-based FPGAs

- *Michinishi, H.; Yokohira, T.; Okamoto, T.; Inoue, T.; Fujiwara, H.*
Dept. of Inf. Technol., Okayama Univ., Japan

This Paper Appears in :
Test Symposium, 1996., Proceedings of the Fifth Asian

on Pages: 68 - 74

This Conference was Held : 20-22 Nov. 1996
1996 ISBN: 0-8186-7478-4
IEEE Catalog Number: 96TB100072
Total Pages: xviii+306
References Cited: 6
Accession Number: 5565434
Abstract:
In this paper we consider testing for programmable interconnect structures of look-up table based FPGAs. The interconnect structure considered in the paper consists of interconnecting wires and programmable points (switches) to join them. As fault models, stuck-at faults of the wires, and extra-device faults and missing-device faults of the programmable points are considered. We heuristically derive test procedures for the faults and then show their validness and complexity.

An approach for detecting multiple faulty FPGA logic blocks

- *Wei Kang Huang; Meyer, F.J.; Lombardi, F.*
Syst. State Key Lab., Fudan Univ., Shanghai, China

This Paper Appears in :
Computers, IEEE Transactions on
on Pages: 48 - 54

Jan. 2000 Vol. 49 Issue: 1 ISSN: 0018-9340
References Cited: 8
CODEN: ITCOB4
Accession Number: 6509362
Abstract:
An approach is proposed to test FPGA logic blocks, including part of the configuration memories used to control them. The proposed AND tree and OR tree-based testing structure is simple and the conditions for constant testability can easily be satisfied. Test generation for only a single logic block is sufficient. We do not assume any particular fault model. Any number of faulty blocks in the chip can be detected. Members of the Xilinx XC3000, XC4000, and XC5200 families were

studied. The proposed AND/OR approach was found to reduce the number of FPGA reprogrammings needed for testing by up to a factor of seven versus direct methods of multiple faulty block detection.

An approach for testing programmable/configurable field programmable gate arrays

- *Huang, W.K.; Lombardi, F.*
Dept. of Comput. Sci., Texas A&M Univ., College Station, TX, USA

This Paper Appears in :
VLSI Test Symposium, 1996., Proceedings of 14th

on Pages: 450 - 455

This Conference was Held : 28 April-1 May 1996
1996 ISBN: 0-8186-7304-4
IEEE Catalog Number: 96TB100043
Total Pages: xxix+510
References Cited: 7
Accession Number: 5391484
Abstract:

This paper presents a new general technique for testing field programmable gate arrays (FPGAs) by fully exploiting their programmable and configurable characteristics. A hybrid fault model is introduced based on a physical and behavioral characterization; this permits the detection of a single fault, as either a stuck-at or a functional fault. A general approach which regards testing as can application for the reconfigurable FPGA, is then proposed. It is shown that different arrangements of disjoint one-dimensional arrays with unilateral horizontal connections and common vertical input lines provide a very good solution. A further feature that is considered for array testing, is the relation between the configuration of the logic blocks and the number of I/O pins in the chip. As an example, the proposed approach is applied for testing the Xilinz 4000 family of FPGAs.

An architecture independent test methodology for SRAM FPGAs

- *Bhullar, G.S.; Szwarc, V.; Kwasniewski, T.A.*
Editor(s): Thorburn, P., Quaicoe, J.
Dept. of Electron., Carleton Univ., Ottawa, Ont., Canada

This Paper Appears in :
Electrical and Computer Engineering, 1997. Engineering Innovation: Voyage of Discovery. IEEE 1997 Canadian Conference on
on Pages: 736 - 739 vol.2

This Conference was Held : 25-28 May 1997
1997 Vol. 2 ISBN: 0-7803-3716-6
IEEE Catalog Number: 97TTH8244
Total Pages: 2 vol. (xxxi+895)
References Cited: 1
Accession Number: 5760399
Abstract:

The effective utilization of FPGAs in the implementation of reconfigurable circuits is contingent on the logic and routing integrity of the devices. To assure this integrity, a means of detecting and localizing logic and routing resource faults is required. This paper presents an architecture independent methodology for testing logic and routing resources of SRAM FPGAs. The proposed methodology employs a functional level device model for the implementation of architecture independent algorithms that allow dynamic generation of test configurations. The flexible device model allows integration of logic and routing resource testing while enhancing the applicability of the test methodology to a broad range of device architectures and sizes.

Minimizing the number of test configurations for different FPGA families

- Renovell, M.; Portal, J.M.; Figuras, J.; Zorian, Y.
LIRMM, Univ. des Sci. et Tech. du Languedoc, Montpellier, France

This Paper Appears in :
Test Symposium, 1999. (ATS '99) Proceedings. Eighth Asian

on Pages: 363 - 368

This Conference was Held : 16-18 Nov. 1999
1999 ISBN: 0-7695-0315-2
Total Pages: xix+406
References Cited: 10
Accession Number: 6544195
Abstract:
This paper describes an approach to minimize the number of test configurations for testing the logic cells of a RAM-based FPGA. The proposed approach is applied to the XILINX SPARTAN, 4000 and 3000 families. On these examples of FPGA, a bottom-up test technique is first used to generate test configurations for the elementary modules, then for a single logic cell, and finally for the m/spl times/m array of logic cells. In this bottom-up technique, it is shown that the key point is the minimization of the number of test configurations for a single logic cell. An approach is then described to define a minimum number of test configurations for a logic cell knowing the test configurations of its logic modules. This approach gives only 4 test configurations for the XILINX Spartan, 5 for the 4000 and 4 for the 3000 while the previous published works concerning Boolean testing of these FPGA families give 8 for the 4000 and 5 for the 3000.

Reconfigurable FPGA's dual role: in-system test and system level logic

- Rosenberg, J.
Atmel Corp., San Jose, CA, USA

This Paper Appears in :
Northcon/94 Conference Record

on Pages: 226 - 229

This Conference was Held : 11-13 Oct. 1994
1994 ISBN: 0-7803-9995-1
Total Pages: vi+392
References Cited: 0

Accession Number: 5093291

Abstract:
Static RAM based field programmable gate arrays (FPGAs) solve the overhead problem because they can be reconfigured in-system any number of times. This unique capability allows the same device to perform a variety of functions without increasing board space or power or sacrificing system performance. When the system is powered up, a special diagnostic configuration can be loaded into the FPGA and test vectors can be applied to the device. Once circuit and board integrity are verified, another configuration file can be loaded into the SRAM cells of the FPGA. Subsequent configuration files can contain any number of logic configurations for the device, enabling it to perform system-level functions. With some thought and creativity, any SRAM FPGA can be configured to test itself. As more and more engineers incorporate on-chip diagnostics into their FPGA designs, self-testing applications will become more sophisticated. This paper explores the dual role of reconfigurable FPGAs in-system: system level logic functions and in-system diagnostics.

SRAM-based FPGA's: testing the interconnect/logic interface

- *Renovell, M.; Portal, J.M.; Figueras, J.; Zorian, Y.*
LIRMM-UM2, Montpellier, France

This Paper Appears in :
Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian

on Pages: 266 - 271

This Conference was Held : 2-4 Dec. 1998
1998 ISBN: 0-8186-8277-9
IEEE Catalog Number: 98TB100259
Total Pages: xviii+528
References Cited: 21
Accession Number: 6294677
Abstract:
This paper address the problem of testing the configurable modules that interface the global interconnect and the logic cells of SRAM-based FPGAs. The Configurable Interface Modules (CIMs) are assumed to be implemented with FPGA multiplexers but the results can be easily extended to any type of interface module. First, it is demonstrated that an address bit Configurable Interface Multiplexer requires N=2/sup n/ test configurations considering a stuck-at as well as a functional fault model. Second, a logic cell with a set of k input Configurable Interface Modules with n address bits is analysed and it is proven that the set of CIMs can be tested in parallel making the number of required test configurations equal to N=2/sup n/. Third, it is shown that the complete circuit, i.e. a m/spl times/m array of sets of k Configurable Interface Multiplexers with n address bits can be tested with only N=2/sup n/ test configurations using the XOR tree and shift register structures.

Test of RAM-based FPGA: methodology and application to the interconnect

- *Renovell, M.; Figueras, J.; Zorian, Y.*
This Paper Appears in :
VLSI Test Symposium, 1997., 15th IEEE

on Pages: 230 - 237

This Conference was Held : 27 April-1 May 1997
1997 ISBN: 0-8186-7810-0
IEEE Catalog Number: TB100125
Total Pages: xxxii+466
References Cited: 25
Accession Number: 5671998
Abstract:

This paper proposes a methodology for testing RAM-based FPGA taking into account the configurability of such flexible devices. Two different approaches with different objectives are identified: the Manufacturing Test Procedure and the User Test Procedure. The proposed method is used to generate a Manufacturing Test Procedure targeting the Interconnect Structure of RAM-based FPGA. It is demonstrated that a set of only 3 Test Configurations called the Orthogonal, the Diagonal-1 and Diagonal-2 Test Configurations suffice to make 100% of the considered realistic fault set non-redundant. Then the test of each configuration is shown equivalent to the test of classical buses. The final proposed Manufacturing Test Procedure present a constant number of Test Configurations (3) and very short Test Sequences.

Testing Carry Logic Modules of SRAM-based FPGAs

Xiaoling Sun, Jian Xu
Dept. of ECE, University of Alberta

The carry logic module (CLM) is an integral part of a configurable logic block (CLB) in a Xilinx XC4000 field programmable gate array (FPGA). This paper addressed the testing issues of a CLM for the first time. The integrity of a CLM is a validated by the integrity of all its components. It has been found that the minimum numbers of CLM test configurations (TCs) under single stuck-at, multiple, stuck-at, and universal fault models are six, seven and eight respectively. A set of selection criteria was proposed to obtain the ‘best’ of eight TCs, each contains a subset of six and seven TCs for the two stuck-at fault models. These CLM TCs can be extended to include the test of the whole CLB.

FPGA Test Time Reduction Through a Novel Interconnect Testing Scheme

Stuart McCracken, Zeljko Zilic
Department of ECE, McGill University
As device densities increase, testing cost is becoming a larger portion of the overall FPGA manufacturing cost. We present an approach to speed up testing FPGA interconnect by reconfiguring it during the test. Simple additions are made to create feedback shift register structures, which considerably reduce the number of test configurations for the switching matrix interconnect. This new testing architecture reduces switching matrix test time by 66% and the diagnosis time by 72%. The additions are transparent to the users both in terms of speed and functionality.

SRAM-based FPGA's: testing the LUT/RAM modules

- *Renovell, M.; Portal, J.M.; Figueras, J.; Zorian, Y.*
LIRMM-UM2, Montpellier, France

This Paper Appears in :
Test Conference, 1998. Proceedings., International

on Pages: 1102 - 1111

This Conference was Held : 18-23 Oct. 1998
1998 ISBN: 0-7803-5093-6
IEEE Catalog Number: 98CH36270
Total Pages: xvi+1179
References Cited: 25
Accession Number: 6265642
Abstract:

This paper addresses the problem of testing the LUT/RAM modules of configurable SRAM-based FPGAs using a minimum number of test configurations. A model of architecture for the LUT/RAM module with N inputs and 2/sup N/ memory cells is proposed taking into account the LUT and RAM modes. Concerning the RAM mode, we demonstrate that a unique test configuration is required for a single module. The problem is shown equivalent to the test of a classical SRAM circuit allowing to use existing algorithms such as the march tests. We also propose a unique test configuration called 'pseudo shift register' for mxm arrays of modules. In this configuration, the circuit operates as a shift register and an adapted version of the MATS++ algorithm called 'shifted MATS++' is described. Concerning the LUT mode, we use the concept of non-redundant test that proposes to test in LUT mode the parts of the module not tested in RAM mode. Under this hypothesis, it is demonstrated that the test of a single module as well as the test of an mxm array of modules require only 3 test configurations. Using our solution, the test of a complete array of mxm LUT/RAM modules requires 4 test configurations independently of the size of the array and of the modules.

Diagnosis

On the complexity of universal fault diagnosis for look-up table FPGAs

Inoue, T. Miyazaki, S. Fujiwara, H.
Graduate Sch. of Inf. Sci., Nara Inst. of Sci. & Technol.;
This paper appears in: Test Symposium, 1997. (ATS '97) Proceedings., Sixth Asian
11/17/1997 -11/19/1997, 17-19 Nov 1997
Location: Akita , Japan
On page(s): 276-281
17-19 Nov 1997
References Cited: 13
Number of Pages: xv+418
INSPEC Accession Number: 5855603
Abstract:
In this paper, we introduce universal fault diagnosis such that when applied to an unprogrammed FPGA, it locates a fault in any faulty programmed FPGA corresponding to the unprogrammed FPGA. If a faulty part in an FPGA can be identified prior to programming it, we can implement a required logic function on the fault-free part by isolating the faulty part. Then, we propose a universal fault diagnosis procedure that locates a faulty CLB in a look-up table FPGA. The complexity of the universal diagnosis procedure for FPGAs with block-sliced loading is independent of its array size, i.e., C-diagnosable

Minimizing the number of programming steps for diagnosis of interconnect faults in FPGAs

Yinlei Yu Jian Xu Wei Kang Huang Lombardi, F.

ASIC State Key Lab., Fudan Univ., Shanghai;
This paper appears in: Test Symposium, 1999. (ATS '99) Proceedings. Eighth Asian
11/16/1999 -11/18/1999, 1999
Location: Shanghai , China
On page(s): 357-362
1999
References Cited: 9
Number of Pages: xix+406
INSPEC Accession Number: 6544194
Abstract:
This paper presents a procedure to diagnose single faults in SRAM based FPGAs. The procedure is nonadaptive and requires six programming steps to give the exact position and type of any single fault in a FPGA. It is proved that the number of programming steps required for the procedure is minimal for a non-adaptive procedure with the given interconnect model

Fault detection and fault diagnosis techniques for lookup table FPGA's

Shyue-Kung Lu Chung-Yang Chen
This paper appears in: Test Symposium, 2002. (ATS '02). Proceedings of the 11th Asian
On page(s): 236- 241
2002
ISSN: 1081-7735
Abstract:
In this paper, we present a novel fault detection and fault diagnosis technique for Field Programmable Gate Arrays
(FPGAs). The cell is configured to implement a bijective function to simplify the testing of the whole cell array. The
whole chip is partitioned into disjoint one-dimensional arrays of cells. The input patterns can be easily generated with a k-bit binary counter. According to the characteristic of bijective cell function, a novel built-in self-test structure is also proposed. To locate a faulty CLB, two diagnosis sessions are required. However, the maximum number of configurations is k + 4 for diagnosing a faulty CLB. The diagnosis complexity of our approach is also analyzed. Our results show that the time complexity is independent of the array size of the FPGA. In other words, we can make the FPGA array C-diagnosable with our approach.

Testing and Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures

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Abstract
As IC densities are increasing, cluster-based FPGA architectures are becoming the architecture of choice for major FPGA manufacturers. A cluster-based architecture is one in which several logic blocks are grouped together into a coarse-grained logic block. While the high density local interconnect often found within clusters serves to improve FPGA utilization, it also greatly complicates the FPGA interconnect testing problem. To address this issue, we have developed a hierarchical approach to define a set of FPGA configurations which enable interconnect fault detection and diagnosis. This technique enables the detection of bridging faults involving intra-cluster interconnect and extra-cluster interconnect. The hierarchical structure of a

cluster-based tile is exploited to define intra-cluster configurations separately from extra-cluster configurations, thereby improving the efficiency of the configuration definition process. The cornerstone of this work is the concise expression of the detectability conditions of each fault, and the distinguishability conditions of each fault pair. By guaranteeing that both intra-cluster and extra-cluster configurations have several test transparency properties, hierarchical fault detectability is ensured.

Diagnosis of interconnect faults in cluster-based FPGA architectures

Authors
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Russell Tessier University of Massachusetts at Amherst

Sponsors
: The IEEE Computer Society DATC
: IEEE Circuits & Systems Society
SIGDA : ACM Special Interest Group on Design Automation

Publisher
IEEE Press Piscataway, NJ, USA

Pages: 472 - 476 Series-Proceeding-Section-Article
Year of Publication: 2000
ISBN:0-7803-6448-1

ABSTRACT

Fault diagnosis has particular importance in the context of field programmable gate arrays (FPGAs) because faults can be avoided by reconfiguration at almost no real cost. Cluster-based FPGA architectures, in which several logic blocks are grouped together into a coarse-grained logic block, are rapidly becoming the architecture of choice for major FPGA manufacturers. The high density interconnect found within clusters greatly complicates the problem of FPGA diagnosis. We propose a technique for the testing and diagnosis of cluster-based FPGA architectures. We present a hierarchical approach to define a set of FPGA configurations in which each fault is detectable, and each fault pair is differentiable. The cornerstone of this work is the concise expression of the distinguishing conditions of each fault pair. Experimental results demonstrate that nearly 100% fault coverage and diagnostic resolution are achieved with a low number of test configurations.

A high resolution diagnosis technique for open and short defects in FPGA interconnects

Author
Mehdi Baradaran Tahoori Stanford University, Stanford, CA

Sponsors
ACM : Association for Computing Machinery
SIGADA : ACM Special Interest Group on Ada Programming Language

Publisher
ACM Press New York, NY, USA

Pages: 248 - 248 Series-Proceeding-Section-Article
Year of Publication: 2003
ISBN:1-58113-651-X

ABSTRACT

A two-step diagnosis flow, coarse-grain and fine-grain, is presented in order to identify a faulty element in the FPGA interconnects. The fault models used for interconnect are open, resistive-open, and bridging fault. The coarse-grain phase identifies the faulty net, the routing between two consecutive sequential elements in the FPGA. This phase is performed by just post-processing tester results for the test configurations used for interconnect testing. During the fine-grain step, the faulty net is rerouted without using some of the resources used in the original routing. The faulty element, programmable switch or wire segment, is uniquely identified based on the tester output for the rerouted configurations. Effective search methods are exploited in order to minimize the number of test configurations and the total diagnosis time. This method is implemented on real FPGA chips and verified using hardware fault emulation.

An automatic testing and diagnosis for FPGAs

- *Doumar, A.; Ito, H.*
Graduate Sch. of Sci. & Technol., Chiba Univ., Japan

This Paper Appears in :
Dependable Computing, 1999. Proceedings. 1999 Pacific Rim International Symposium on

on Pages: 45 - 52

This Conference was Held : 16-17 Dec. 1999
1999 ISBN: 0-7695-0371-3
Total Pages: xii+277
References Cited: 19
Accession Number: 6461655

Abstract:
This paper presents a new design for testing and diagnosing the SRAM-based field programmable gate arrays (FPGA). By slightly modifying the original FPGA's SRAM memory, the new architecture permits the configuration data to be looped on a chip. Then the full testing and diagnosing of the FPGA are achieved by loading typically only one testing configuration datum (carefully chosen) instead of loading the total required configurations data (which is a very slow process) in the normal cases. Other configurations data are obtained by shifting the first one inside the chip. Consequently the test becomes faster. This method does not need a large outside memory (off-chip memory) for the test. The evaluation proves that this method becomes very interesting when the complexity of the configurable blocks (CLBs) or the chip size increase.

Diagnosing single faults for interconnects in SRAM based FPGAs

- *Yinlei Yu; Jian Xu; Wei Kang Huang; Lombardi, F.*
ASIC & Syst. State Key Lab., Fudan Univ., Shanghai, China

This Paper Appears in :

Design Automation Conference, 1999. Proceedings of the ASP-DAC '99. Asia and South Pacific

on Pages: 283 - 286 vol.1

This Conference was Held : 18-21 Jan. 1999
1999 ISBN: 0-7803-5012-X
IEEE Catalog Number: 99EX198
Total Pages: (xxvi+372+suppl.)
References Cited: 6
Accession Number: 6358304
Abstract:
This paper presents a method to diagnose faults in FPGA interconnection resources. A single fault model is given. Under the given model, a diagnosing method is proposed. At most five programming steps in the proposed method is required if adaptive testing scheme is used. For non-adaptive test, eight programming steps is required to diagnose all the possible faults under the given single fault model. The accuracy of the fault diagnosing is one segment for a segment stuck-at or stuck-open fault, a segment pair for a bridge fault, a switch for switch stuck-on or stuck-off fault.

Fault detection and location of dynamic reconfigurable FPGAs

- *Chi-Feng Wu; Cheng-Wen Wu*
Dept. of Electr. Eng., Nat. Tsing Hua Univ., Hsinchu, Taiwan

This Paper Appears in :
VLSI Technology, Systems, and Applications, 1999. International Symposium on
on Pages: 215 - 218

This Conference was Held : 8-10 June 1999
1999 ISBN: 0-7803-5620-9
IEEE Catalog Number: 99TH8453
Total Pages: xi+305
References Cited: 10
Accession Number: 6504371

Abstract:
Dynamic reconfigurable FPGAs provide a platform for reconfigurable computing as well as fast prototyping and emulation. For such FPGAs, we propose a dynamic serial (DS) test approach which takes advantage of their dynamic reconfiguration feature for testing. Compared with the parallel approach, the DS test approach significantly reduces the test configuration time and requires less I/O pins, resulting in a faster and easier testing procedure for dynamic reconfigurable FPGAs.

Test and diagnosis of faulty logic blocks in FPGAs

- *Wang, S.-J.; Tsai, T.-M.*
Inst. of Comput. Sci., Nat. Chung-Hsing Univ., Taichung, Taiwan

This Paper Appears in :
Computers and Digital Techniques, IEE Proceedings-

on Pages: 100 - 106

March 1999 Vol. 146 Issue: 2 ISSN: 1350-2387
References Cited: 11
CODEN: ICDTEA
Accession Number: 6296042
Abstract:
Field programmable gate arrays (FPGAs) have been used in many areas of digital design. Because FPGAs are programmable, faults in them can be easily tolerated once fault sites are located. However, diagnosis of faults in FPGA has not yet been explored by researchers. A new methodology for the testing and diagnosis of faults in FPGAs is presented, based on built-in self-test. The proposed method imposes no hardware overhead, and requires minimal support from external test equipment. Test time depends only on the number of faults, and is independent of the chip size. With the help of this technique, chips with faults can still be used. As a result, the chip yield can be improved and chip cost is reduced. This method can also be used in fault-tolerant systems, in which a good functional circuit can still be mapped to a FPGA with faulty elements, as long as the fault sites are known.

Diagnosis of Open Defects in FPGA Interconnect
Mehdi Baradaran Tahoori
Stanford University

In this paper, we present coarse-grain and fine-grain diagnosis techniques to identify a faulty element in FPGA interconnects. The fault model we use is stuck-open and resistive-open for interconnects. The presented technique requires only a small number of configurations while offering high resolution diagnosis. We implemented this technique on real FPGA chips and verified it using fault emulation.

Built-In Self Test

Built-in self-test of logic blocks in FPGAs (Finally, a free lunch: BIST without overhead!)

Stroud, C. Konala, S. Ping Chen Abramovici, M.
Dept. of Electr. Eng., Kentucky Univ., Lexington, KY;
This paper appears in: VLSI Test Symposium, 1996., Proceedings of 14th
04/28/1996 -05/01/1996, 28 Apr-1 May 1996
Location: Princeton, NJ , USA
On page(s): 387-392
28 Apr-1 May 1996
References Cited: 14
INSPEC Accession Number: 5391475
Abstract:
We present a new approach for Field Programmable Gate Array (FPGA) testing that exploits the reprogrammability of FPGAs to create Built-In Self-Test (BIST) logic only during off-line test. As a result, BIST is achieved without any area overhead or performance penalties to the system function implemented by the FPGA. Our approach is applicable to all levels of testing, achieves maximal fault coverage, and all tests are applied at-speed. We describe the BIST architecture used to test all the programmable logic blocks in an FPGA and the configurations required to implement our approach using a commercial FPGA. We also discuss implementation problems caused by CAD
tool limitations and limited architectural resources, and we describe techniques which overcome these limitations

Built-in self-test of FPGA interconnect

Stroud, C.   Wijesuriya, S.   Hamilton, C.   Abramovici, M.
Dept. of Electr. Eng., Kentucky Univ., Lexington, KY;
This paper appears in: Test Conference, 1998. Proceedings. International
10/18/1998 -10/23/1998, 18-23 Oct 1998
Location: Washington, DC ,   USA
On page(s): 404-411
18-23 Oct 1998
References Cited: 15
Number of Pages: xvi+1179
INSPEC Accession Number: 6251471
Abstract:
We introduce the first BIST approach for testing the programmable routing network in FPGAs. Our method detects opens in, and shorts among, wiring segments, and also faults affecting the programmable switches that configure the FPGA interconnect. As a result, the BIST technique provides complete testing of interconnect faults

Using ILA testing for BIST in FPGAs

Stroud, C.   Lee, E.   Konala, S.   Abramovici, M.
Dept. of Electr. Eng., Kentucky Univ., Lexington, KY;
This paper appears in: Test Conference, 1996. Proceedings., International
10/20/1996 -10/25/1996, 20-25 Oct 1996
Location: Washington, DC ,   USA
On page(s): 68-75
20-25 Oct 1996
References Cited: 23
Number of Pages: xii+951
INSPEC Accession Number: 5539829
Abstract:
We present an improved Built-In Self-Test (BIST) approach for the programmable logic blocks (PLBs) of a Field Programmable Gate Array (FPGA), which repeatedly reconfigures the FPGA as a group of C-testable iterative logic arrays. The new architecture is easily scalable with increasing size of FPGAs and ensures routability of the various configurations required to completely test the FPGA in three test sessions. In addition, the BIST approach addresses RAM mode testing as well as testing the adder/subtractor modes in FPGAs

Self-testing of S-compatible test units in user-programmed FPGAs

Tomaszewicz, P.   Krasniewski, A.
Inst. of Telecommun., Warsaw Univ. of Technol. ;
This paper appears in: EUROMICRO Conference, 1999. Proceedings. 25th
09/08/1999 -09/10/1999, 1999
Location: Milan ,   Italy
On page(s): 254-259 vol.1
Volume: 1,   1999
References Cited: 7
Number of Pages: 2 vol. (xxviii+530+478)
INSPEC Accession Number: 6364136
Abstract:
A method for the development of a test plan for BIST based exhaustive testing of a circuit implemented with an in-system reconfigurable FPGA is presented. A test plan for application-dependent testing of an FPGA is based on the concept of a logic cone. Logic cones that satisfy single-generator compatibility requirement can be combinationally-exhaustively tested concurrently and are merged into a test block. The number of test blocks corresponds to the number of test sessions. For the presented algorithm of computing logic

cones, a tool was developed. The presented experimental results are used to develop heuristic rules that control the logic cone merging process

Boundary scan access of built-in self-test for field programmable gate arrays

- *Gibson, G.; Gray, L.; Stroud, C.*
Editor(s): Mukund, P.R., Sridhar, R., Gabara, T., Carothers, J.D.
Dept. of Electr. Eng., Kentucky Univ., Lexington, KY, USA

This Paper Appears in :
ASIC Conference and Exhibit, 1997. Proceedings., Tenth Annual IEEE International
on Pages: 57 - 61

This Conference was Held : 7-10 Sept. 1997
1997 ISBN: 0-7803-4283-6
IEEE Catalog Number: 97TH8334
Total Pages: xix+370
References Cited: 10
Accession Number: 5774208

Abstract:
We discuss issues associated with system level access of Built-In Self-Test (BIST) for Field Programmable Gate Arrays (FPGAs) via the Boundary Scan Interface. In addition, we describe the design of an Application Specific Integrated Circuit (ASIC) which serves as an interface between a PC parallel port and the Test Access Port (TAP) of one or more FPGAs to reprogram the FPGA(s) and administer BIST during off-line testing. We also include a brief description of the FPGA BIST architecture and operation.

Built-in self-test for multiple CLB faults of a LUT type FPGA

- *Itazaki, N.; Matsuki, F.; Matsumoto, Y.; Kinoshita, K.*
Dept. of Appl. Phys., Osaka Univ., Japan

This Paper Appears in :
Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian

on Pages: 272 - 277

This Conference was Held : 2-4 Dec. 1998
1998 ISBN: 0-8186-8277-9
IEEE Catalog Number: 98TB100259
Total Pages: xviii+528
References Cited: 4
Accession Number: 6288503
Abstract:
A new Built-in Self Test (BIST) method for multiple configurable logic block (CLB) faults of SRAM-Look-Up-Table (LUT) type FPGA is reported. In this method, self test is performed concurrently for every test block containing eight CLBs. Faulty FPGA which includes up to five faulty CLBs in one test block can be detected completely even if each faulted CLB includes unlimited number of faults.

Methods for boundary scan access of built-in self-test for field programmable gate arrays

- *Hamilton, C.; Wijesuriya, S.; Gibson, G.; Stroud, C.*
Dept. of Electr. Eng., Kentucky Univ., Lexington, KY, USA

This Paper Appears in :
Southeastcon '99. Proceedings. IEEE

on Pages: 210 - 216

This Conference was Held : 25-28 March 1999
1999 ISBN: 0-7803-5237-8
IEEE Catalog Number: 99CH36300
Total Pages: xiii+341
References Cited: 9
Accession Number: 6422210

Abstract:

In this paper we present four methods for accessing BIST for FPGAs via the IEEE 1149.1 standard boundary scan interface along with the advantages and disadvantages of each approach. Each method is evaluated with consideration to test time, logic overhead, diagnostics resolution, usability in FPGAs, and architectural features which would be required to implement the approach. These methods can be used in a variety of FPGA architectures for all levels of testing.

Selecting built-in self-test configurations for field programmable gate arrays

- *Stroud, C.; Lee, E.; Konala, S.; Abramovici, M.*
Dept. of Electr. Eng., Kentucky Univ., Lexington, KY, USA

This Paper Appears in :
AUTOTESTCON '96, Test Technology and Commercialization. Conference Record

on Pages: 29 - 35

This Conference was Held : 16-19 Sept. 1996
1996 ISBN: 0-7803-3379-9
IEEE Catalog Number: 96CH35955
Total Pages: 488
References Cited: 11
Accession Number: 5526485

Abstract:
In our previous work, we have described a built-in self-test (BIST) approach for RAM-based field programmable gate arrays (FPGAs), which exploits the reprogrammability of the FPGA to create BIST logic only during off-line testing. The cost is additional external memory required to store the BIST reconfiguration data, leaving all FPGA logic resources available for system functions. In this paper, the memory requirements as well as the testing time are minimized by selecting a few BIST configurations which provide high fault coverage for inspection tests at board and system manufacturing as well as for efficient system diagnostics and field testing.

Novel Technique for Built-In-Self-Test of FPGA Interconnects

Xiaoling Sun, Jian Xu, Ben Chan
Dept. of ECE, University of Alberta

This paper presents the first BIST approach for testing interconnects of SRAM-based FPGAs using error control coding. The proposed scheme requires a total of six test configurations and has superior multiple fault coverage on wire segment stuck-at, stuct-open and bridging faults, programmable switch stuck on/off faults, and the combinations of these faults in global routing resources

Design and Implementation of a Parity-Based BIST Scheme For FPGA Global Interconnects

Xiaoling Sun, Susan Xu and Jian Xu
Dept. of ECE, University of Alberta

This paper presents the design and implementation of a parity-based built-in self-test (BIST) scheme for interconnects of field programmable gate arrays (FPGAs). The self-test is achieved by using a set of proposed test configurations (TCs). Design flows were developed to enable the implementation. We utilized the exisiting features of FPGA design tools and developed a tool to automate the required interconnect routing. The conventional FPGA design flow was used to implement the BIST circuitry. A complete FPGA TC was presented. The pre- and post-mapping simulations were conducted. The results validate the feasibility of the proposed in-system testing scheme.

Minimal Test Configurations for FPGA Local Interconnects

X. Sun, J, Xu and A. Alimohammad
Department of ECE, University of Alberta

This paper presents a built-in self-test (BIST) technique for testing local interconnects of Field Programmable Gate Arrays (FPGAs). To maximize the parallel testing, we use error control coding to test one portion of interconnects and functional test of D flip-flops to verify the integrity of another portion of interconnects in a test configuration (TC). We introduce a heuristic method for deriving minimal interconnect TCs by modeling local interconnects with adjacency graphs, then solving the graph coloring problems. The proposed scheme has superior multiple fault coverage.

BIST-based diagnosis of FPGA interconnect

Stroud, C. Nall, J. Lashinsky, M. Abramovici, M.
Dept. of Electr. & Comput. Eng., North Carolina Univ., Charlotte, NC, USA;
This paper appears in: Test Conference, 2002. Proceedings. International
On page(s): 618- 627
2002
ISSN: 1089-3539
Number of Pages: xvi+1250
INSPEC Accession Number: 7528831
Abstract:
We present a Built-In Self-Test (BIST)-based diagnostic approach for the programmable interconnect resources in Field Programmable Gate Arrays (FPGAs) that can be used for either on-line or off-line testing. The technique was originally intended for on-line diagnosis of faulty interconnect to support fault-tolerant applications. However, the technique has been proven to be an excellent approach for off-line testing and diagnosis
as well, providing high-resolution diagnostics with the ability to identify the faulty wire segment or programmable switch. We have implemented this BIST-based diagnostic approach on the ORCA series FPGA and present the results of testing and diagnosing known defective FPGAs.

BIST-based test and diagnosis of FPGA logic blocks

Abramovici, M. Stroud, C.E.

Lucent Technol., Murray Hill, NJ;
This paper appears in: Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
On page(s): 159-172
Volume: 9, Issue: 1, Feb 2001
ISSN: 1063-8210
References Cited: 43
CODEN: IEVSE9
INSPEC Accession Number: 6938201
Abstract:
We present a built-in self-test (BIST) approach able to detect and accurately diagnose all single and practically all multiple faulty programmable logic blocks (PLBs) in field programmable gate arrays (FPGAs) with maximum diagnostic resolution. Unlike conventional BIST, FPGA BIST does not involve any area overhead or performance degradation. We also identify and solve the problem of testing configuration multiplexers that was either ignored or incorrectly solved in most previous work. We introduce the first diagnosis method for multiple faulty PLBs; for any faulty PLB, we also identify its internal faulty modules or modes of operation. Our accurate diagnosis provides the basis for both failure analysis used for yield improvement and for any repair strategy used for fault-tolerance in reconfigurable systems. We present experimental results showing detection and identification of faulty PLBs in actual defective FPGAs. Our BIST architecture is easily scalable

Enhanced BIST-based diagnosis of FPGAs via boundary scan access

Hamilton, C. Gibson, G. Wijesuriya, S. Stroud, C.
Dept. of Electr. Eng., Kentucky Univ., Lexington, KY;
This paper appears in: VLSI Test Symposium, 1999. Proceedings. 17th IEEE
04/25/1999 -04/29/1999, 1999
Location: Dana Point, CA , USA
On page(s): 413-418
1999
References Cited: 6
IEEE Catalog Number: PR00146
Number of Pages: xxxii+488
INSPEC Accession Number: 6450991
Abstract:
Four methods for accessing BIST for FPGAs via the IEEE 1149.1 standard boundary scan interface are presented and discussed in terms of advantages/disadvantages including their impact on test time and diagnostic resolution. These methods can be used in a variety of FPGA architectures for system level testing and diagnosis

Built-in self-test and fault diagnosis for lookup table FPGAs

Shyue-Kung Lu Jen-Sheng Shih Cheng-Wen Wu
Dept. of Electron. Eng., Fu Jen Catholic Univ., Taipei;
This paper appears in: Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on
05/28/2000 -05/31/2000, 2000
Location: Geneva , Switzerland
On page(s): 80-83 vol.1
Volume: 1, 2000
References Cited: 13
Number of Pages: 5 vol.(viii+813+768+769+768+760)
INSPEC Accession Number: 6703597
Abstract:
A novel built-in self-test structure for the lookup table (LUT) based field programmable gate arrays (FPGA's) is proposed in this paper. A general structure for the basic configurable logic array blocks (CLB's) is assumed. The whole chip is partitioned into disjoint one-dimensional arrays of cells. We assume that in each linear array, there is at most one faulty

cell, and a faulty cell may contain multiple faulty CLB's. Our idea is to configure the cells to make each cell function bijective. In order to detect all faults defined, k+2 configurations are required. The input patterns can be easily generated with a k-bit counter and the fault coverage is 100%. The number of configurations for our BIST structures is 2k+4. Our BIST approaches also have the advantages of requiring less hardware resources for test pattern generation and output response analysis. To locate a faulty CLB, three test sessions are required. However, the maximum number of configurations is k+4 for diagnosing a faulty CLB.

BIST-based detection and diagnosis of multiple faults in FPGAs

Abramovici, M.   Stroud, C.
Lucent Technol. Bell Labs., Murray Hill, NJ;
This paper appears in: Test Conference, 2000. Proceedings. International
10/03/2000 -10/05/2000, 2000
Location: Atlantic City, NJ ,   USA
On page(s): 785-794
2000
References Cited: 36
Number of Pages: xiv+1158
INSPEC Accession Number: 6859167
Abstract:
We present a BIST-based approach able to detect and accurately diagnose any single and most multiple faulty programmable logic blocks (PLBs) in field programmable gate arrays (FPGAs). For any faulty PLB, we also identify its internal faulty modules or modes of operation. This accurate diagnosis provides the basis for both failure analysis used for yield improvement and for any repair strategy used for fault-tolerance. We present experimental results showing detection and identification of faulty PLBs in actual defective FPGAs

BIST-based diagnostics of FPGA logic blocks

Stroud, C.   Lee, E.   Abramovici, M.
Dept. of Electr. Eng., Kentucky Univ., Lexington, KY;
This paper appears in: Test Conference, 1997. Proceedings., International
11/01/1997 -11/06/1997, 1-6 Nov 1997
Location: Washington, DC ,   USA
On page(s): 539-547
1-6 Nov 1997
References Cited: 19
Number of Pages: xiv+1054
INSPEC Accession Number: 5863282
Abstract:
Accurate diagnosis is an essential requirement in many testing environments, since it is the basis for any repair or replacement strategy used for chip or system fault-tolerance. In this paper we present the first approach able to diagnose faulty programmable logic blocks (PLBs) in Field Programmable Gate Arrays (FPGAs) with maximal diagnostic resolution. Our approach is based on a new Built-In Self-Test (BIST) architecture for FPGAs and can accurately locate any single and most multiple faulty PLBs. An adaptive diagnostic strategy provides identification of faulty PLBs with a 7% increase in testing time over the complete detection test, and can also be used for manufacturing yield enhancement. We present results showing identification of faulty PLBs in defective ORCA chips

Design For Testability

IS-FPGA : a new symmetric FPGA architecture with implicit scan

Renovell, M.   Faure, P.   Portal, J.M.   Figueras, J.   Zorian, Y.
LIRMM-UM2, Montpellier;
This paper appears in: Test Conference, 2001. Proceedings. International
10/30/2001 -11/01/2001, 2001

Location: Baltimore, MD , USA
On page(s): 924-931
2001
References Cited: 18
IEEE Catalog Number: 01CH37260
Number of Pages: xiv+1201
INSPEC Accession Number: 7211392
Abstract:
Proposes a new and original FPGA architecture with testability facilities. It is first demonstrated that classical FPGA architectures do not allow one to efficiently implement sequential circuits with a scan chain. It is consequently proposed to modify the architecture of classical FPGAs in order to create an implicit-scan chain into the FPGA itself called implicit scan FPGA (IS-FPGA). Using this new FPGA architecture, any sequential circuit implemented into the FPGA is 'implicitly scanned'. An original and optimal implementation of the proposed architecture is given with minimum area overhead and absolutely no delay impact. Additionally the technique is transparent for the user as well as for the FPGA mapping tools. Finally, it is demonstrated that the implicit-scan concept allows 'over-scan' of sequential circuits resulting in highly testable circuits

A row-based FPGA for single and multiple stuck-at fault detection

Chen, X.T. Huang, W.K. Lombardi, F. Sun, X.
Dept. of Comput. Sci., Texas A&M Univ., College Station, TX;
This paper appears in: Defect and Fault Tolerance in VLSI Systems, 1995. Proceedings., 1995 IEEE International Workshop on,
11/13/1995 -11/15/1995, 13-15 Nov 1995
Location: Lafayette, LA , USA
On page(s): 225-233
13-15 Nov 1995
References Cited: 10
INSPEC Accession Number: 5262081
Abstract:
This paper presents a practical and low cost design-for-testability (DFT) scheme for the row-based field programmable gate array (FPGA) which is widely used for rapid prototyping, hardware verification/emulation of VLSI chips and manufacturing of complex digital systems. A new module is introduced for the DFT of the FPGA. The proposed DFT scheme permits the uncommitted FPGA to be tested using a set of constant cardinality (C-testability) for single and multiple stuck-at fault detection, while reducing the number of required primary test pins to only one. The number of tests for the FPGA is still $8+n_f$ (where n_f is the number of sequential modules in a row of the array), but only one primary pin and a small amount of testing circuitry are now required. This paper also modifies the single fault test set to accomplish multiple fault detection under two multiple fault models: the multiple fault single module (MFSM) and the single fault multiple module (SFMM) models. It is shown that by appropriately changing the don't care entries in the vectors of the test set for single fault detection, 100% and nearly 100% fault coverages can be achieved under the MFSM and SFMM models respectively

Testing the logic cells and interconnect resources for FPGAs

Doumar, A. Ito, H.
Dept. of Inf. & Comput. Sci., Chiba Univ.;
This paper appears in: Test Symposium, 1999. (ATS '99) Proceedings. Eighth Asian
11/16/1999 -11/18/1999, 1999
Location: Shanghai , China
On page(s): 369-374
1999
References Cited: 9

Number of Pages: xix+406
INSPEC Accession Number: 6544196
Abstract:
This paper presents a new design for testing SRAM based field programmable gate arrays (FPGAs). The new proposed method is able to test both the configurable logic blocks (CLBs) and the interconnection networks. The proposed design is based on slightly modifying the original SRAM part in the FPGA so that it will allow the configuration data to be looped on a chip and then the test becomes easier. This method requires a very short test time compared to the previous works. Moreover, the off-chip memory used in the storage of the configurations data is considerably reduced. The application of this method to the XC4000 family and ORCA shows that (relative to that required by the previous works) the test time can be reduced by 87.2% and the required off-chip memory can be reduced by 88.6%

FPGA Delay Fault Testing

Testing FPGA delay faults in the system environment is very different from "ordinary" delay fault testing

Krasniewski, A.
Inst. of Telecommun., Warsaw Univ. of Technol. ;
This paper appears in: On-Line Testing Workshop, 2001. Proceedings. Seventh International
07/09/2001 -07/11/2001, 2001
Location: Taormina , Italy
On page(s): 37-40
2001
References Cited: 20
Number of Pages: xi+228
INSPEC Accession Number: 7120133
Abstract:
Explains differences between testing delay faults in FPGAs and testing delay faults in circuits whose combinational sections can be represented as gate networks. Formulates - in a form suitable for analysis of LUT-based FPGAs - conditions that allow one to check whether or not a given input pair is a test of specific type (non-robust, robust, etc.). The presented theoretical results are shown to simplify an analysis of the various methods for enhancing the effectiveness of detection of FPGA delay faults

Evaluation of delay fault testability of LUT functions for improved efficiency of FPGA testing

Krasniewski, A.
Inst. of Telecommun., Warsaw Univ. of Technol. ;
This paper appears in: Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on
09/04/2001 -09/06/2001, 2001
Location: Warsaw , Poland
On page(s): 310-317
2001
References Cited: 26
Number of Pages: xii+476
INSPEC Accession Number: 7081959

Abstract:
Testing delay faults in FPGAs differs significantly from testing delay faults in circuits whose combinational sections can be represented as gate networks. Based on delay fault testability conditions, formulated in a form suitable for analysis of LUT-based FPGAs, we develop an original method for the evaluation of delay fault testability of LUT functions. It relies on an indicator called delay fault activation profile. The proposed method supports an analysis and comparison of different procedures for the enhancement of detectability of FPGA delay faults that rely on transformations of user-defined functions of LUTs in the combinational logic block under test. We demonstrate the effectiveness of our method by applying it to prove the efficiency and to optimize a specific procedure for the transformation of LUT functions which preserves the blocking capability and input-output transition pattern of original functions

Self-testing of FPGA delay faults in the system environment

Krasniewski, A.
Inst. of Telecommun., Warsaw Univ. of Technol. ;
This paper appears in: On-Line Testing Workshop, 2000. Proceedings. 6th IEEE International
07/03/2000 -07/05/2000, 2000
Location: Palma de Mallorca , Spain
On page(s): 40-41
2000
References Cited: 7
IEEE Catalog Number: 99TH8471
Number of Pages: x+220
INSPEC Accession Number: 6722228
Abstract:
We propose a procedure for self-testing of an FPGA programmed to implement a user-defined function. The procedure is intended to improve the detectability of FPGA delay faults. This improvement is obtained by modifying the functions of LUTs in the section under test, so that each LUT implements a XOR function. We show that, despite many potential problems, the proposed modification can significantly enhance the susceptibility of FPGA delay faults to random testing

BIST-based delay-fault testing in FPGAs

Abramovici, M. Stroud, C.
Circuits & Syst. Res. Lab., Agere Syst., Murray Hill, NJ, USA;
This paper appears in: On-Line Testing Workshop, 2002. Proceedings of the Eighth IEEE International
On page(s): 131- 134
2002
ISSN:
Number of Pages: xiv+273
INSPEC Accession Number: 7425817
Abstract:
We present the first delay-fault testing approach for FPGAs, applicable both for manufacturing and for on-line testing. Our approach is based on BIST, is comprehensive, and does not require expensive ATE. We have successfully implemented this BIST approach on the ORCA 2C series FPGA.

Application-dependent testing of FPGA delay faults

Krasniewski, A.
Inst. of Telecommun., Warsaw Univ. of Technol. ;
This paper appears in: EUROMICRO Conference, 1999. Proceedings. 25th
09/08/1999 -09/10/1999, 1999
Location: Milan , Italy
On page(s): 260-267 vol.1
Volume: 1, 1999

References Cited: 22
Number of Pages: 2 vol. (xxviii+530+478)
INSPEC Accession Number: 6364137
Abstract:
To ensure correct operation of an FPGA based system with regard to timing characteristics, an application-dependent FPGA testing, i.e. testing of an FPGA programmed to implement a user-defined function, must be performed. We propose a procedure for application-dependent self testing of an in-circuit reprogrammable FPGA and develop BIST schemes that preserve the FPGA timing. For these schemes, the reconfiguration of a portion of the FPGA into test resources has no impact on the timing characteristics of that part of the FPGA which is currently being tested. We also present a method for enhancing the susceptibility of FPGA delay faults to random testing. It is based on modifying the functions of programmable logic components in the section under test. We compare the efficiency of the self-test scheme that uses this method with the earlier reported BIST techniques that rely on the design of test pattern generators best suited for pseudoexhaustive testing of delay faults

Self-testing of FPGA delay faults in the system environment

Krasniewski, A.
Inst. of Telecommun., Warsaw Univ. of Technol. ;
This paper appears in: On-Line Testing Workshop, 2000. Proceedings. 6th IEEE International
07/03/2000 -07/05/2000, 2000
Location: Palma de Mallorca , Spain
On page(s): 40-41
2000
References Cited: 7
IEEE Catalog Number: 99TH8471
Number of Pages: x+220
INSPEC Accession Number: 6722228
Abstract:
We propose a procedure for self-testing of an FPGA programmed to implement a user-defined function. The procedure is intended to improve the detectability of FPGA delay faults. This improvement is obtained by modifying the functions of LUTs in the section under test, so that each LUT implements a XOR function. We show that, despite many potential problems, the proposed modification can significantly enhance the susceptibility of FPGA delay faults to random testing

Evaluation of delay fault testability of LUT functions for improved efficiency of FPGA testing

Krasniewski, A.
Inst. of Telecommun., Warsaw Univ. of Technol. ;
This paper appears in: Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on
09/04/2001 -09/06/2001, 2001
Location: Warsaw , Poland
On page(s): 310-317
2001
References Cited: 26
Number of Pages: xii+476
INSPEC Accession Number: 7081959
Abstract:
Testing delay faults in FPGAs differs significantly from testing delay faults in circuits whose combinational sections can be represented as gate networks. Based on delay fault testability conditions, formulated in a form suitable for analysis of LUT-based FPGAs, we develop an original method for the evaluation of delay fault testability of LUT functions. It relies on an indicator called delay fault activation profile. The proposed method supports an analysis and

comparison of different procedures for the enhancement of detectability of FPGA delay faults that rely on transformations of user-defined functions of LUTs in the combinational logic block under test. We demonstrate the effectiveness of our method by applying it to prove the efficiency and to optimize a specific procedure for the transformation of LUT functions which preserves the blocking capability and input-output transition pattern of original functions

Improving Detectability of Resistive Open Defects in FPGA

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Stanford University, Stanford, CA 94305

This paper presents a new technique for detecting resistive open defects in FPGAs. This technique is based on the reconfigurability feature of FPGAs. Using this technique, the detectability of the defect can be improved by several orders of magnitude. Also, a method is developed to scale the detectability. Simulation results show the effectiveness of this method.

Testing for Resistive Open Defects in FPGAs
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This paper presents a new technique for detecting resistive open defects in FPGAs. This technique is based on the reconfigurability feature of FPGAs. Using this technique, the delay of a defective path is increased several times more than the delay of the fault-free path, resulting in a higher resolution in detectability of resistive open defects in FPGAs, even at lower tester speed. Various detailed SPICE simulations are performed to validate this method. Also, a test configuration generation scheme is presented for the entire FPGA.

Test Pattern Generation/Fault Grading

TOF: a tool for test pattern generation optimization of an FPGA application oriented test

Renovell, M. Portal, J.M. Faure, P. Figueras, J. Zorian, Y.
LIRMM-UM2, Montpellier;
This paper appears in: Test Symposium, 2000. (ATS 2000). Proceedings of the Ninth Asian
12/04/2000 -12/06/2000, 2000
Location: Taipei , Taiwan
On page(s): 323-328
2000
References Cited: 16
Number of Pages: xxiii+495
INSPEC Accession Number: 6846346
Abstract:
The objective of this paper is to generate an Application-Oriented Test Procedure to be used by a FPGA user in a given application. General definitions concerning the specific problem of testing RAM-based FPGAs are first given such as the important concept of `AC-non-redundant fault.” Then, it is commented that a classical test pattern generation performed on the circuit netlist gives a low AC-non-redundant fault coverage and it is pointed out that test pattern generation performed on a FPGA representation is required. It is also commented that test pattern generation performed on the FPGA representation can be significantly

accelerated by different techniques. A procedure called TOF is described to validate the proposed approach on benchmark circuits

Fault grading FPGA interconnect test configurations

Tahoori, M.B. Mitra, S. Toutounchi, S. McCluskey, E.J.
Center for Reliable Comput., Stanford Univ., CA, USA;
This paper appears in: Test Conference, 2002. Proceedings. International
On page(s): 608- 617
2002
ISSN: 1089-3539
Number of Pages: xvi+1250
INSPEC Accession Number: 7528830
Abstract:
Conventional fault simulation techniques for FPGAs are very complicated and time consuming. The other alternative, FPGA fault emulation technique, is incomplete, and can be used only after the FPGA chip is manufactured. In this paper, we present efficient algorithms for computing the fault coverage of a given FPGA test configuration. The faults considered are opens and shorts in FPGA interconnects. Compared to conventional methods, our technique is orders of magnitude faster, while is able to report all detectable and undetectable faults.

Effects of technology mapping on fault-detection coverage in reprogrammable FPGAs

- *Kwiat, K.; Debany, W.; Hariri, S.*
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This Paper Appears in :
Computers and Digital Techniques, IEE Proceedings-

on Pages: 407 - 410

Nov. 1995 Vol. 142 Issue: 6 ISSN: 1350-2387
References Cited: 9
CODEN: ICDTEA
Accession Number: 5120829

Abstract:
Although field-programmable gate arrays (FPGAs) are tested by their manufacturers prior to shipment, they are still susceptible to failures in the field. In this paper test vectors generated for the emulated (i.e. mission) circuit are fault-simulated on two different models: the original view of the circuit, and the design as it is mapped to the FPGA's logic cells. Faults in the cells and in the programming logic are considered. Experiments show that this commonly-used approach fails to detect most of the faults in the FPGA.

Test pattern and test configuration generation methodology for the logic of RAM-based FPGA

- *Renovell, M.; Portal, J.M.; Figueras, J.; Zorian, Y.*
LIRMM, Montpellier, France

This Paper Appears in :
Test Symposium, 1997. (ATS '97) Proceedings., Sixth Asian

on Pages: 254 - 259

This Conference was Held : 17-19 Nov. 1997
1997 ISBN: 0-8186-8209-4
IEEE Catalog Number: 97TB100205
Total Pages: xv+418
References Cited: 17
Accession Number: 5849190

Abstract:

The test of the Configurable Logic Blocks of RAM based FPGAs under a Stuck-At fault model has been studied. The high cost of changing the configuration, by reprogramming the FPGA during testing, forces a strategy to reduce the number of different configurations used for testing purposes. After finding the optimal solutions for the elementary structures of the Logic block, Multiplexers and Look-Up Tables, the problem of testing interconnected elementary structures is addressed. The method is illustrated using an elementary structure and then applied to a popular FPGA (XILINX 3000 family) where a reduced set of configurations (5) and their corresponding test sequences is found to cover all (100%) the Configurable Logic Block faults modelled.

Analyzing the test generation problem for an application-oriented test of FPGAs

Renovell, M. Portal, J.M. Faure, P. Figueras, J. Zorian, Y.
LIRMM-UM2, Montpellier;
This paper appears in: European Test Workshop, 2000. Proceedings. IEEE
05/23/2000 -05/26/2000, 2000
Location: Cascais , Portugal
On page(s): 75-80
2000
References Cited: 12
Number of Pages: xii+181
INSPEC Accession Number: 6788969
Abstract:
The objective of this paper is to generate an application-oriented test procedure to be used by a FPGA user in a given application. General definitions concerning the specific problem of testing RAM-based FPGAs are first given such as the important concept of `AC-non-redundant fault'. Using a set of circuits implemented on a XILINX 4000E, it is shown that a classical test pattern generation performed on the circuit netlist gives a low AC-non-redundant fault coverage and it is pointed out that test pattern generation performed on a FPGA representation is required. It is then demonstrated that test pattern generation performed on the FPGA representation can be significantly accelerated by removing most of the AC-redundant faults. Finally, a technique is proposed to even more accelerate the test pattern generation process by using a reduced FPGA description

A novel fault injection method for system verification based on FPGA boundary scan architecture

Chakraborty, T.J. Chen-Huan Chiang
Lucent Technol. Bell Labs., Whippany, NJ, USA;
This paper appears in: Test Conference, 2002. Proceedings. International
On page(s): 923- 929
2002
ISSN: 1089-3539
Number of Pages: xvi+1250
INSPEC Accession Number: 7534875

Abstract:
A novel fault injection (a.k.a. fault insertion) method to facilitate the development of high quality system test is presented in this paper In this method, we utilize the existing boundary scan (BS) architecture of an FPGA to inject a hardware fault condition at any pin of the FPGA on a circuit board. Existing user-defined instructions of most FPGA BS architectures and the newly proposed design of their corresponding user-defined scan registers (USRs) constitute the proposed fault injection architecture. No new instruction, and no modification of the existing test access port (TAP) controller and BS registers are required. In addition, it is possible to reconfigure where and what type of faults to be injected asynchronously via the BS architecture while the system is online. Although the proposed method incurs at least additional delay through a multiplexer on the pin where a fault is injected, the programmability of an FPGA enables us to add fault injection logic only to where fault injection function is desired. Hence, area overhead and performance impact can be significantly reduced.

Fault Models

A new functional fault model for FPGA application-oriented testing

Rebaudengo, M.   Reorda, M.S.   Violante, M.
Politecnico di Torino;
This paper appears in: Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 17th IEEE International Symposium on
On page(s): 372- 380
2002
ISSN: 1063-6722
Abstract:
The objective of this paper is to propose a new fault model suitable for test pattern generation for an FPGA configured to implement a given application. The paper demonstrates that the faults affecting the bit cells of the Look-Up Tables (LUTs) are not redundant, although they store constant values. We demonstrate that these faults cannot be neglected and that the fault model corresponding to modifying the content of each LUT memory cell must be considered in order to cover the full range of possible faults. In order to evaluate the fault coverage of the proposed fault model, a set of circuits mapped on a Xilinx Virtex 300 FPGA have been considered. Test sequences generated by a gate-level commercial ATPG and an academic RT-level one have been fault simulated on these benchmark circuits. The obtained figures show that a high percentage of faults affecting the LUT bit cells are undetected, thus suggesting that suitable ATPG algorithms adopting the new fault model are required.

Modeling of FPGA local/global interconnect resources and derivation of minimal test configurations

Sun, X.   Alimohammad, A.   Trouborst, P.
University of Alberta;
This paper appears in: Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 17th IEEE International Symposium on
On page(s): 284- 292
2002
ISSN: 1063-6722

Abstract:
Not Available

On fault modeling and fault tolerance of antifuse based FPGAs

- *Roy, K.*
Texas Instruments, Inc., Dallas, TX, USA

This Paper Appears in :
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on

on Pages: 1623 - 1626 vol.3

This Conference was Held : 3-6 May 1993
May 1993 ISBN: 0-7803-1281-3
Total Pages: 4 Vols., 2829
References Cited: 3
Accession Number: 4996964
Abstract:
The fault modeling, fault location, and fault tolerance of antifuse-based field programmable gate arrays (FPGAs) are discussed. The antifuse faults are divided into two categories, i.e., those that can be detected before programmation, and those that can be detected only after programmation. It is shown that some of the antifuse open and short faults may also appear as delay faults. The redundancy inherent in the FPGAs is utilized fully to achieve fault tolerance without extra circuitry.

Online Testing

On-line testing of transient and crosstalk faults affecting interconnections of FPGA-implemented systems

Metra, C. Pagano, A. Ricco, B.
Dipt. di Elettronica, Inf. e Sistemistica, Bologna Univ.;
This paper appears in: Test Conference, 2001. Proceedings. International
10/30/2001 -11/01/2001, 2001
Location: Baltimore, MD , USA
On page(s): 939-947
2001
References Cited: 29
IEEE Catalog Number: 01CH37260
Number of Pages: xiv+1201
INSPEC Accession Number: 7211394
Abstract:
In this paper we propose a self-checking scheme for the on-line testing of transient and crosstalk faults affecting the interconnections of synchronous systems implemented using Field-Programmable Gate-Arrays (FPGAs). An FPGA prototype has been implemented, whose correct operation has been verified by means of post-layout simulations and experimental measurements

Roving STARs: an integrated approach to on-line testing, diagnosis, and fault tolerance for FPGAs in adaptive computing systems

Abramovici, M. Emmert, J.M. Stroud, C.E.
Circuits & Syst. Res. Lab., Agere Syst., Murray Hill, NJ;
This paper appears in: Evolvable Hardware, 2001. Proceedings. The Third NASA/DoD Workshop on
07/12/2001 -07/14/2001, 2001
Location: Long Beach, CA , USA

On page(s): 73-92
2001
References Cited: 58
Number of Pages: x+287
INSPEC Accession Number: 7024508
Abstract:
We present an integrated approach to on-line FPGA testing, diagnosis and fault tolerance, to be used in high-reliability and high-availability hardware. The testing and diagnostic process takes place in Self-Testing AReas (STARs) of the FPGA, without disturbing the normal system operation. The entire chip is tested by roving the STARs across the FPGA. Our approach guarantees complete testing of both logic cells and interconnect with maximum diagnostic resolution. Our multi-level fault-tolerant technique allows using partially defective logic and routing resources for normal operation, providing longer mission life in the presence of faults. In addition, our dynamic fault-tolerant method ensures that spare resources are always present in the neighborhood of the located fault, thus simplifying fault-bypassing. Our complete method has been successfully implemented and demonstrated on the ORCA 2CA series FPGAs from Lucent Technologies

Using roving STARs for on-line testing and diagnosis of FPGAs in fault-tolerant applications

Abramovici, M.   Strond, C.   Hamilton, C.   Wijesuriya, S.   Verma, V.
Bell Labs., Lucent Technol., Murray Hill, NJ;
This paper appears in: Test Conference, 1999. Proceedings. International
09/28/1999 -09/30/1999, 1999
Location: Atlantic City, NJ ,   USA
On page(s): 973-982
1999
References Cited: 33
Number of Pages: xiv+1163
INSPEC Accession Number: 6536453
Abstract:
In this paper we present a novel integrated approach to on-line FPGA testing, diagnosis, and fault-tolerance, to be used in high-reliability and high-availability hardware. The test process takes place in self-testing areas (STARs) of the FPGA, without disturbing the normal system operation. The entire chip is eventually tested by having (STARs) gradually rove across the FPGA. Our approach guarantees complete testing of programmable logic blocks and interconnect, and provides maximum diagnostic resolution. A new fault-tolerant (FT) technique allows using partially defective FPGA resources for normal operation, providing longer mission life-span in the presence of faults. We also introduce the basic concepts of a new dynamic FT method, spare resources needed to bypass a fault are always in the neighborhood of the located fault, thus simplifying fault-bypassing
technique allows using partially defective FPGA resources for normal operation, providing

Improving on-line BIST-based diagnosis for roving STARs

Abramovici, M.   Stroud, C.   Skaggs, B.   Emmert, J.
Lucent Technol. Bell Labs., Murray Hill, NJ;
This paper appears in: On-Line Testing Workshop, 2000. Proceedings. 6th IEEE International
07/03/2000 -07/05/2000, 2000
Location: Palma de Mallorca ,   Spain
On page(s): 31-39
2000
References Cited: 26
IEEE Catalog Number: 99TH8471
Number of Pages: x+220
INSPEC Accession Number: 6722227

Abstract:
We present improvements to our on-line BIST-based diagnosis technique originally used in the roving STARs approach. The enhanced technique starts with a new method of analyzing the BIST results, and employs the original divide-and-conquer method as a second phase only when the first phase fails or it does not achieve maximum diagnostic resolution. The combined technique significantly reduces the diagnosis time, improves the resolution in several cases, and also requires less fault-free resources

On-line BIST and diagnosis of FPGA interconnect using roving STARs

Stroud, C.   Lashinsky, M.   Nall, J.   Emmert, J.   Abramovici, M.
Dept. of Electr. & Comput. Eng., North Carolina Univ., Charlotte, NC;
This paper appears in: On-Line Testing Workshop, 2001. Proceedings. Seventh International
07/09/2001 -07/11/2001, 2001
Location: Taormina ,   Italy
On page(s): 27-33
2001
References Cited: 19
Number of Pages: xi+228
INSPEC Accession Number: 7120131
Abstract:
Presents the first on-line BIST and BIST-based diagnostic approach for the programmable interconnect resources in FPGAs. This interconnect BIST is used in the roving STARs approach. The technique provides a complete BIST of the programmable interconnect followed by high-resolution diagnostics to support reconfiguration around the fault for fault-tolerant applications. We have successfully implemented this BIST approach on the ORCA 2C series FPGA and present the results of testing and diagnosing known defective FPGAs

Active replication: towards a truly SRAM-based FPGA on-line concurrent testing

Gericota, M.G.   Alves, G.R.   Silva, M.L.   Ferreira, J.M.
Dept. of Electr. Eng., ISEP, Porto, Portugal;
This paper appears in: **On-Line Testing Workshop, 2002. Proceedings of the Eighth IEEE International**
On page(s): 165- 169
2002
ISSN:
Number of Pages: xiv+273
INSPEC Accession Number: 7425823

Abstract:
The reusing of the same hardware resources to implement speed-critical algorithms, without interrupting system operation, is one of the main reasons for the increasing use of reconfigurable computing platforms, employing complex SRAM-based FPGAs. However, new semiconductor manufacturing technologies increase the probability of lifetime operation failures, requiring new on-line testing/fault-tolerance methods able to improve the dependability of the systems where they are included. The Active Replication technique presented in this paper consists of a set of procedures that enables the implementation of a truly non-intrusive structural on-line concurrent testing approach, detecting and avoiding permanent faults and correcting errors due to transient faults. In relation to a previous technique proposed by the authors as part of the DRAFT FPGA concurrent test methodology, the Active Replication technique extends the range of circuits that can be replicated, by introducing a novel method with very low silicon overhead.

On-line fault detection for bus-based field programmable gate arrays

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Dept. of Electr. Eng. & Comput. Sci., MIT, Cambridge, MA, USA

This Paper Appears in :
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on

on Pages: 656 - 666

Dec. 1998 Vol. 6 Issue: 4 ISSN: 1063-8210
References Cited: 29
CODEN: IEVSE9
Accession Number: 6126397

Abstract:
We introduce a technique for on-line built-in self-testing (BIST) of bus-based field programmable gate arrays (FPGAs). This system detects deviations from the intended functionality of an FPGA without using special-purpose hardware, hardware external to the device, and without interrupting system operation. Such a system would be useful for mission-critical applications with resource constraints. The system solves these problems through an on-line fault scanning methodology. A device's internal resources are configured to test for faults. Testing scans across an FPGA, checking a section at a time. Simulation on a model FPGA supports the viability and effectiveness of such a system.

Testing approach within FPGA-based fault tolerant systems

Doumar, A. Ito, H.
Dept. of Inf. & Image Sci., Chiba Univ.;
This paper appears in: Test Symposium, 2000. (ATS 2000). Proceedings of the Ninth Asian
12/04/2000 -12/06/2000, 2000
Location: Taipei , Taiwan
On page(s): 411-416
2000
References Cited: 6
Number of Pages: xxiii+495
INSPEC Accession Number: 6846360
Abstract:
Proposes a test strategy for FPGAs to be applied within FPGA-based fault-tolerant systems. We propose to make some configurable logic blocks (CLBs) under test and to implement the rest of the CLBs with the normal user data. In the target fault-tolerant systems, there are two phases (the functional phase and the test phase). In the functional phase, the system achieves its normal functionality, while in the test phase,
the FPGA is tested. In this phase, the configuration data of the CLBs under test are shifted on-chip in parallel to other CLBs for achieving the test in these CLBs. All the CLBs are tested in a single test phase. The shifting process control, test application and test observation are achieved by the logic managing the fault tolerance (from outside the chip). The system returns to its normal phase after all the CLBs have been scanned by the test. The application of this approach reduces the fault tolerance cost (hardware, software, time, etc). The user is then able to periodically test the chip using only the data inside the chip and without destroying the original configuration data. No particular hardware is required for saving the test data on-board. Additionally, no particular software treatment is required for the test. The testing time is reduced enormously. Unfortunately, as a consequence of implementing two types of data on-chip, a 15% decrease in the chip functionality and a 2.5% delay overhead are noticed in the case of structures similar to a 20×20 Xilinx FPGA