KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 571 Digital System Testing
Syllabus - Term 072

Catalog Description

Issues of VLSI testing, test Economics. Fault models: Transistor level faults, Single and Multiple stuck at faults, Bridging faults, Functional faults, Delay faults. Automatic Test Pattern Generation for Combinational logic: Path sensitization, D-Algorithm, Critical path, PODEM, FAN, CMOS testing. Sequential logic testing. Design for testability. Built-in-self-test (BIST). Functional testing, testing of regular structures, Testability measures. Delay testing. Testing of systems on chip.

Prerequisite: COE 308 and COE 360

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Office Hours SMW 11:00-12:00 PM

Text Book: *Digital Systems Testing and Testable Design, by Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman, IEEE Press, 1990.*

Grading Policy

Assignments	15%
Exam I	15% **(S., March 29, 7:00 PM)**
Exam II	20% **(S., May 17, 7:00 PM)**
Project	20%
Paper Presentations	10%
Final	20%

- Attendance will be taken regularly.
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- Late assignments will be accepted but you will be penalized 10% per each late day.
- A student caught cheating in any of the assignments will get 0 out of 15%.
- No makeup will be made for missing Exams.

Course Topics

1. ***Introduction:*** The testing problem, costs of testing, test types and schemes.
2. ***Fault modeling***: Fault detection and redundancy, fault equivalence, dominance, checkpoints and collapsing. Fault diagnosis. Stuck-at faults, bridging faults, transistor faults, delay faults, etc.
3. ***Fault simulation:*** serial, parallel, deductive, and concurrent fault simulation. Parallel pattern single fault propagation, critical path tracing and fault sampling.
4. ***Test generation for Combinational circuits:*** Boolean difference, path sensitization, D-algorithm, PODEM, and FAN. Random test generation, Combined random/deterministic test generation. Test compaction. Cost functions and testability measures.
5. ***Test generation for sequential circuits***: Time-frame expansion, extended D-algorithm, BACK algorithm, simulation-based approaches, and complexity of sequential ATPG.
6. ***Test generation for CMOS circuits:*** Test generation for transistor stuck-open and stuck short faults. Test generation based on gate-level models, robust and non-robust test generation.
7. ***Delay-fault testing***: Gate and path delay fault models, robust, validatable nonrobust and nonrobust test vectors, path delay fault simulation and test generation.
8. ***Design for testability***: Ad-hoc methods, types of scan cells, LSSD, full scan design, partial scan design, and boundary scan design. Partial scan selection techniques.
9. ***Built-in self test***: Theory and operation of LFSR, MISR, random and weighted random pattern testability, BIST pattern generator and response analyzer, scan-based BIST architecture, and test point insertion for improving random testability.