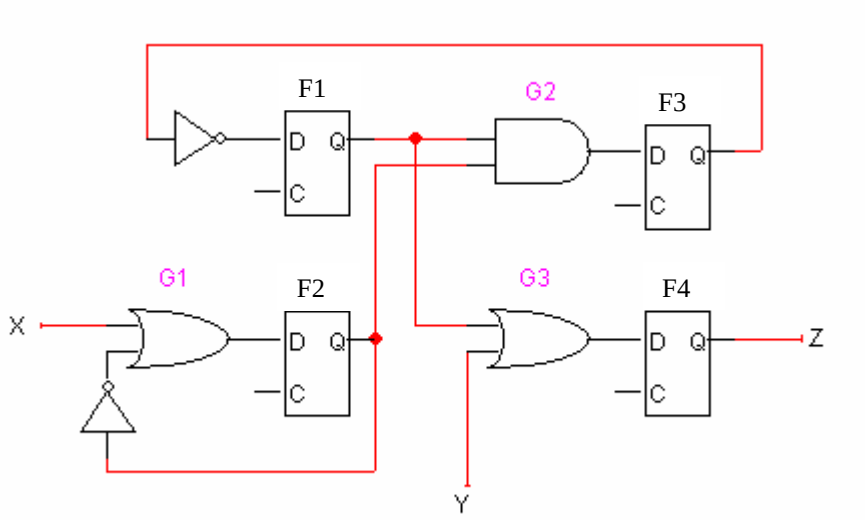
COE 571 Digital System Testing

Term 072

HW# 5

Due date: Wednesday, June 4, 2008

Q.1. Consider the sequential circuit shown below, which has two primary inputs X and Y, and one primary output Z, and four D-FFs:



(i) Convert the circuit into a full-scanned circuit using multiplexed data FF. Then, explain how the fault G2 stuck-at-0 can be detected by the full-scanned circuit.

(ii) Suppose that a partial scan design is to be constructed by scanning a single flip flop. Which of the flip-flops you will select to be scanned? Justify your answer. What type of scan flip flop you will use for partial scan design?

(iii) Assume that to enhance the testability of the circuit, it is required to add an observation point on the Q output of F2, a 0-injection control point on the output of G2, and both a 0 and 1 injection on the output of G3. Modify the design so that it has the desired features such that the control and observation points are driven by a scan register. Assume that during the scan operation, the normal state of the circuit should not be disturbed.

(iv) Show a boundary scan implementation of the circuit including scanning all the flip-flops in the design.

Q.2. Given the characteristic polynomial $p(x)=1+x^2+x^3$:

(i) Is p(x) a primitive polynomial? Justify your answer.

(ii) Show a Type 1 LFSR implementation of p(x), and determine the sequence generated by the LFSR.

(iii) Show a Type 2 LFSR implementation of p(x), and determine the sequence generated by the LFSR.

(iv) Determine the reciprocal polynomial p*(x).

(v) Show a Type 2 LFSR implementation of p*(x), and determine the sequence generated by the LFSR. Verify that it produces the reverse of the sequence generated by the one in (iii).

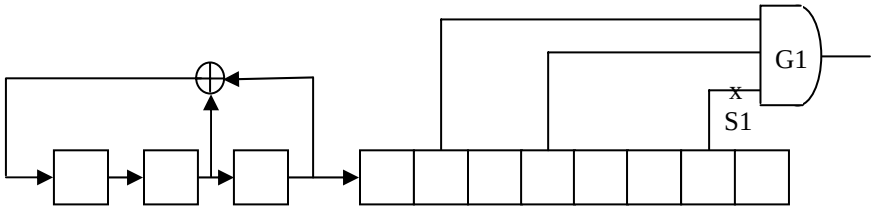
Q.3. Consider a type-2 SISR with characteristic polynomial $p(x)=1+x+x^2$. Suppose that the following fault free output response is generated by a circuit: 10110111. Determine whether the following erroneous output sequences will be detected or not. Justify your answer:

(i) 10110000.

(ii) 10111010.

(iii) 01110111.

Q.4. Consider the circuit shown below, where a 3-stage LFSR is feeding a scan chain of length 8. Assume that the scan chain drives the gate G1 as shown and that G1 is connected to a primary output. Determine whether the indicated single stuck-at fault can be detected by the LFSR or not. If a fault can be detected, determine the seed of the LFSR to generate the test for the fault.



Q.5. OPUS is a partial scan package based on cycle breaking and testability measures. Consider the sequential circuit s15850.bench with 77 inputs, 150 outputs and 534 FFs.

(i) Perform full scan of the circuit using the command ***fullscan*** and determine the fault coverage and CPU time. This command converts scanned FFs into PIs and POs.

(ii) Perform full scan of the circuit using the command ***addmux -scan***. This command adds MUXs to scanned FFs and places them in a single scan chain. Determine the obtained fault coverage and CPU time, and compare them to what you obtained in (i). Comment on your observations.

(iii) Perform partial scan of the circuit scanning 20%, 30%, and 50% using each of the following commands. Compare the fault coverage and CPU time for each case. Use the ***makescan*** command to convert selected FFs to PIs and POs.

One. ***Opus -n -i***

Two. ***Opus -t -i***

Three. ***Opus -t***