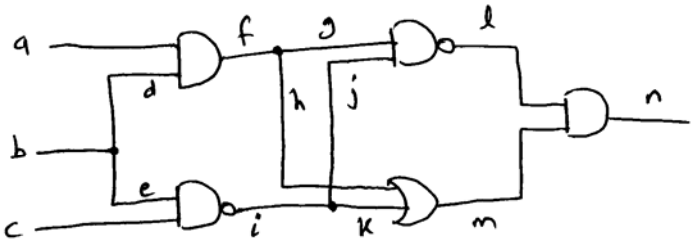
COE 571 Dr. El-Malch

HW #3 Solution

Q1.



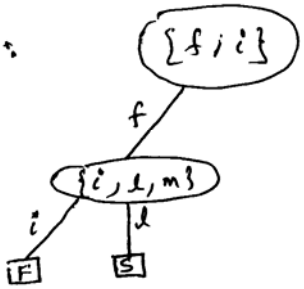
(i) D-Algorithm:

1. b s-a-0:

Decision Sel.	Implication	Comment	D-F	D-F
	b=1, d=D, e=D̄	Activate the fault		{f, i}
a=1	f=D, g=D, h=D	propagate through f		{i, l, m}
c=1	i=D̄, k=D̄, j=D̄, l=1, m=1, n=1	propagate through i Failure		
j=1	i=1, c=0, l=D̄, k=1, m=1, n=D̄	propagate through l success		

Test pattern (abc) = 110.

Decision Tree:

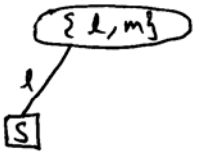


2. d s-a-0 :

Decision Sel.	Implication	Comment	J-F	D-F
	d=1, b=1, e=1 a=1, f=D, g=D, h=D	Activate Fault		{l, m}
j=1	j=1, i=1, c=0, l=D̄, k=1, m=1, n=D̄	propagate thr. l success		

Test pattern (abc) = 110.

Decision Tree :



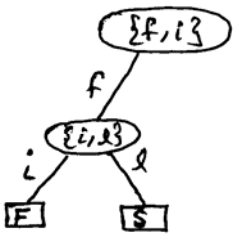
(ii) g-v Algorithm :

1. b s-a-0 :

Decision Sel.	Implication	Comment	J-F	D-F
	b=1, d=D, e=D, f=μ/0, i=μ/1, g=μ/0, h=μ/0, j=μ/1, k=μ/1, l=μ/1, m=μ/1, n=μ/1	Activate Fault		{f, i}
a=1	f=D, g=D, h=D, m=1	Propagate thr. f		{i, l}
c=1	i=D̄, j=D̄, k=D̄, l=1, n=1	Prop. thr. i Failure		
j=1/μ	i=1/μ, c=0, i=1, k=1, j=1, l=D̄, n=D̄	Prop. thr. l success		

Test pattern (abc) = 110

Decision Tree:



2. d s-a-0 :

Decision Sel.	Implication	comment	J-F	D-F
	d=1, b=1, e=1, a=1, f=D, g=D, h=D, l=μ/1, m=1/μ	Activate Fault		{l, m}
j=1/μ	i=1/μ, c=0, i=1, j=1, k=1, m=1, l=$\bar{D}$, n=$\bar{D}$	Prop. thr. l Success		

Test pattern (abc) = 110

Decision Tree:

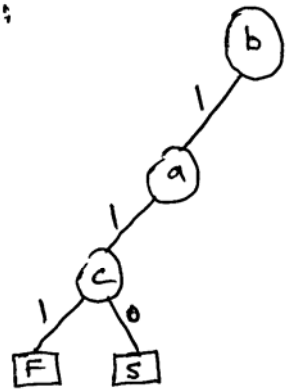
(iii) Podem:

1. b s-a-0:

objective	PI Assignment	Implication	D-F
b = 1	b = 1	d = D, e = D	{f, i}
a = 1	a = 1	f = D, g = D, h = D	{i, l, m}
c = 1	c = 1	i = $\bar{D}$, j = $\bar{D}$, K = $\bar{D}$, l = 1, m = 1, n = 1 (Failure)	
	c = 0	i = 1, j = 1, K = 1, l = $\bar{D}$, m = 1, n = $\bar{D}$ (success	

Test pattern (abc) = 110

Decision Tree:

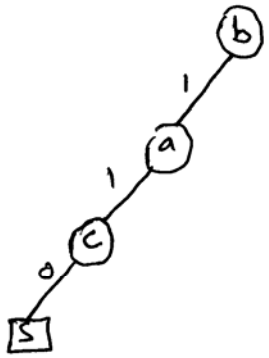


2. d s-a-0 :

objective	PI Assignment	Implication	D-F
$d=1$	$b=1$	$e=1, d=0$	{f}
$a=1$	$a=1$	$f=0, g=0, h=0$	{l, m}
$j=1$	$c=0$	$i=1, k=1, j=1, l=\bar{D}, m=1, n=\bar{D}$ success	

Test pattern (abc) = 110

Decision Tree:



Verification of Generated Tests for parts (i), (ii) and (iii):

Circuit Netlist	**Signal Names**
INPUT(a) INPUT(b) INPUT(c) OUTPUT(n) f = AND(a,b) i = NAND(b,c) l = NAND(f,i) m = OR(f,i) n = AND(l,m) END	1 a 2 b 3 c 4 f 5 i 6 l 7 m 8 n 9 n_$OUTPUT
Fault b s-a-0	Fault d s-a-0
Fault Representation: 2 0 0 Simulated Vector: 110 Detection Status: user time 0.000000 sec sys time 0.000000 sec det faults 1 tot faults 1 coverage 1.000000	Fault Representation: 4 2 0 Simulated Vector: 110 Detection Status: user time 0.000000 sec sys time 0.000000 sec det faults 1 tot faults 1 coverage 1.000000

(iv) Test Generation using HITEC:

Fault b s-a-0	Fault d s-a-0
Fault Representation: 2 0 0 Generated Vector: 011 Note that the test generated is different but it is a valid test. This is due to the choice made in propagating the fault. If the fault effect is propagated across node i first, we will get this test.	Fault Representation: 4 2 0 Generated Vector: 111 Note that the test generated is different but it is a valid test. This is due to the choice made in propagating the fault. If the fault effect is propagated across node m first, we will get this test.