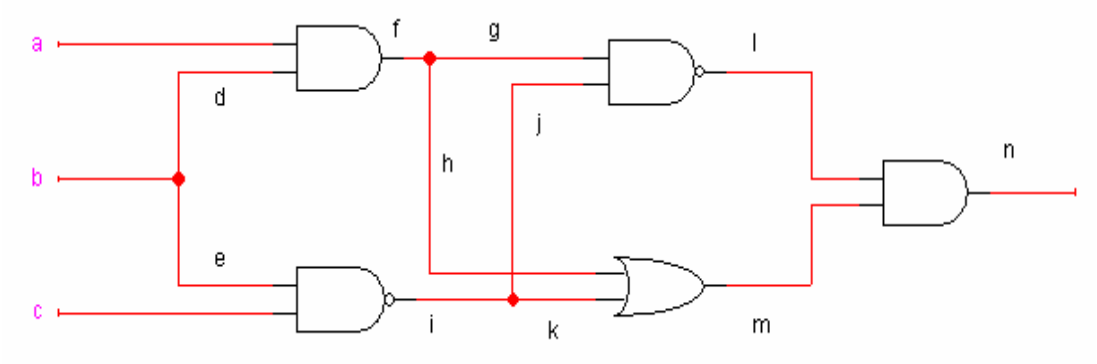
COE 571 Digital System Testing

Term 072

HW# 3

Due date: Monday, April 21

Q.1. Consider the circuit given below. For each of the single stuck-at faults, **b s-a-0** and **d s-a-0,** perform the following:



(i) Generate a test for the considered fault using the **D algorithm**. Show all the details of the algorithm including the D-Frontier, the J-Frontier and the Decision tree. Whenever there are choices, select the choices in ascending alphabetical order. If the fault is detectable, verify your result by fault simulating the derived test using either PROOFS or HOPE.

(ii) Generate a test for the considered fault using the **9-v algorithm**. Show all the details of the algorithm including the D-Frontier, the J-Frontier and the Decision tree. Whenever there are choices, select the choices in ascending alphabetical order. If the fault is detectable, verify your result by fault simulating the derived test using either PROOFS or HOPE.

(iii) Generate a test for the considered fault using the **PODEM algorithm**. Show all the details of the algorithm including the D-Frontier and the Decision tree. Whenever there are choices, select the choices in ascending alphabetical order. If the fault is detectable, verify your result by fault simulating the derived test using either PROOFS or HOPE.

(iv) Generate a test for the considered faults using HITEC and compare the obtained test to your solutions in (i), (ii) and (iii) if the fault is detectable.