COE 571 Digital System Testing

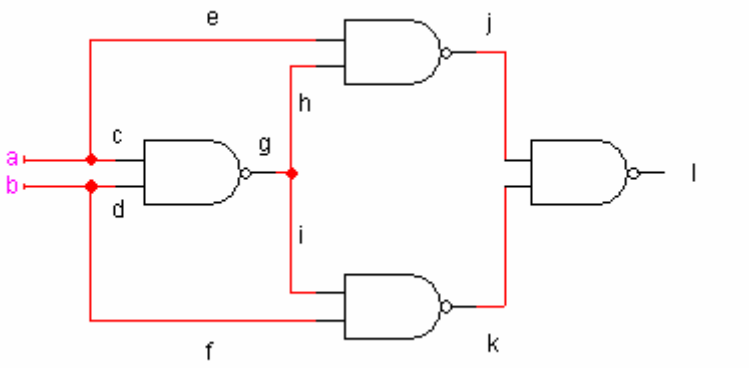
Term 072

HW# 2

Due date: Tuesday, March 25

Q.1. Given a manufacturing process with a certain yield Y=70%. Determine the minimum required fault coverage for achieving a defect level of 1 chip per a 1000. Use the Williams and Brown model and assume that fault coverage is equal to the defect coverage as an approximation.

Q.2. Considering the circuit shown below and the following fault list {a_0, a_1, b_0, b_1, c_1, d_1, g_0, g_1, e_1, h_1, i_1, f_1, j_1, k_1, l_1, l_0}, determine the faults detected by the test vector 11 based on each of the following methods. Show the details of each method.



(i) Deductive fault simulation.

(ii) Critical path tracing.

(iii) Parallel fault simulation.

(iv) Verify your answer of part (ii) using the CPT implementation given in class using the following command: hope –t circuit.hope –C circuit.log –L 7 circuit.bench. Note that circuit.hope is the file containing the test vectors, circuit.log is the file that will contain the results, and circuit.bench is the file containing the circuit.

(v) Verify your answer of parts (i) & (iii) by simulating the given test vector using PROOFS.