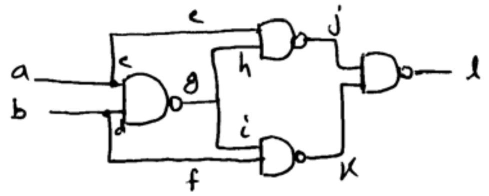
COE 571 Dr. El-Maleh

HW #1 Solution

Q1.



(i)

$$l = \overline{(ab)}\, a + \overline{(ab)} \cdot b$$
$$= (\bar{a} + \bar{b})\, a + (\bar{a} + \bar{b})\, b$$
$$= a\bar{b} + \bar{a} b = a \oplus b$$

In the presence of the fault g s-a-1,

$$l^{g1} = a + b$$

The set of all test vectors that detect the fault g s-a-1 is given by

$$(a \oplus b) \oplus (a + b) = 1$$

$$[\,\bar{a}\,[\,b\,] + a\,[\,\bar{b}\,]\,] \oplus [\,\bar{a}\,[b] + a\,[1]\,] = 1$$

$$\Rightarrow \bar{a}\,[0] + a\,[b] = 1$$

$$\Rightarrow ab = 1$$

Thus, there is only one test vector to detect the fault a=1 and b=1.

(ii) Faulty function is $\bar{a} + \bar{b}$

Set of test vectors to detect the multiple stauck-at fault $\{e$ s-a-1, f s-a-0$\}$ is given by $(a \oplus b) \oplus (\bar{a} + \bar{b}) = 1$

$\Rightarrow \; [\bar{a}[b] + a[\bar{b}]] \oplus [\bar{a}[1] + a[\bar{b}]] = 1$

$\Rightarrow \; [\bar{a}[\bar{b}] + a[0]] = 1$

$\Rightarrow \; \bar{a}\,\bar{b} = 1$

Thus, there is only a single test vector

$a = 0$ and $b = 0$

(iii) AND bridging between lines A and B.

Faulty function $= \overline{(ab \cdot ab)} \cdot ab + \overline{(ab \cdot ab)}\, ab$

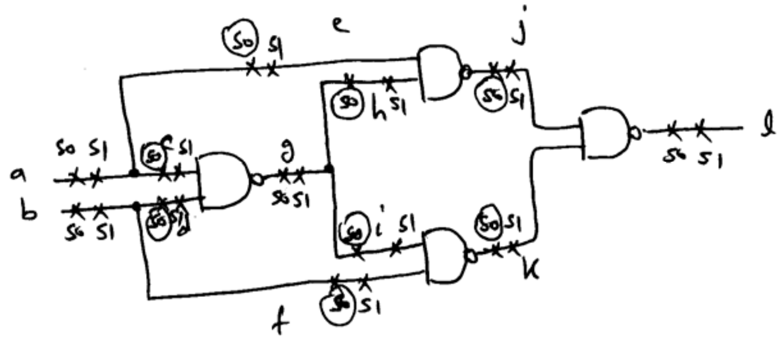
$= \overline{(ab)} \cdot ab + \overline{(ab)}\, ab = 0$

Thus, the set of test vectors that detect the fault is given by

$a \oplus b \oplus 0 = 1 \;\Rightarrow\; a \oplus b = 1$

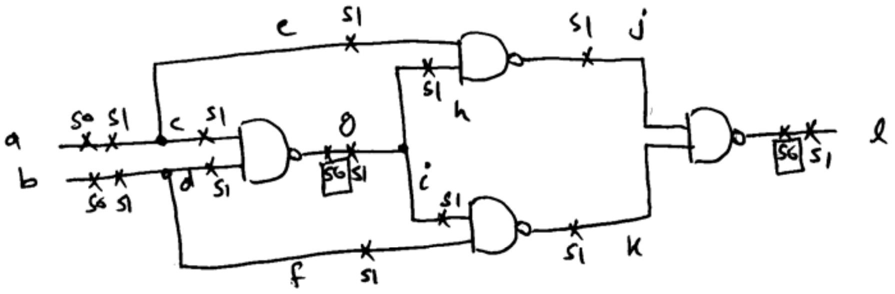
$\Rightarrow \; a = 1$ & $b = 0$ or $a = 0$ & $b = 1$.

(iv)



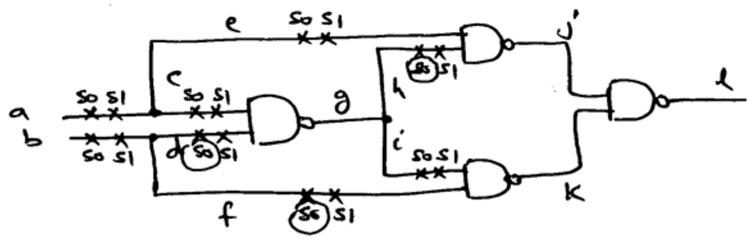
Faults removed due to equivalence relation are circled. Thus, we end up with 16 faults

(v)



Faults that can be removed due to dominance relation are shown in a square. Thus, we end up with 14 faults.

(vi) checkpoint Theorem



Faults removed due to fault equivalence are circled. No faults can be removed due to fault dominance. Thus, we end up with 13 faults.

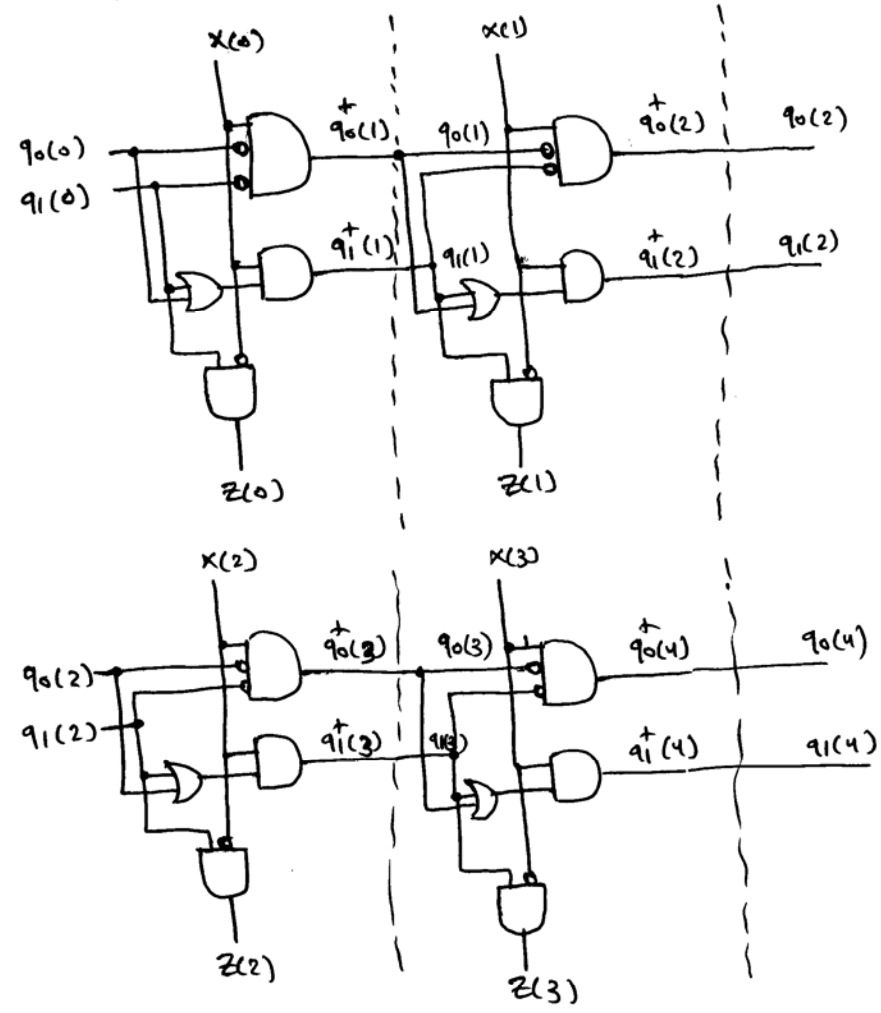
(vii) Fault Collapsing using HITEC:

<table>
<tr><th>Circuit Netlist</th><th>Signal Names</th></tr>
<tr><td>INPUT(a)
INPUT(b)
OUTPUT(l)
g = NAND(a, b)
j = NAND(a, g)
k = NAND(g, b)
l = NAND(j, k)</td><td>1 a
2 b
3 g
4 j
5 k
6 l
7 l_$OUTPUT</td></tr>
<tr><th colspan="2">Collapsed Faults</th></tr>
<tr><td colspan="2">7 0 1 : 7 1 1 : 6 0 1 : 6 2 0 : 5 0 0 : 6 1 0 : 4 0 0 ;
5 2 1 ;
2 0 1 ;
5 1 1 ;
3 0 1 : 3 2 0 : 3 1 0 ;
2 0 0 ;
1 0 0 ;
4 2 1 ;
1 0 1 ;
4 1 1 ;
7 0 0 : 7 1 0 : 6 0 0 ;
6 2 1 : 5 0 1 : 5 2 0 : 5 1 0 ;
3 0 0 ;
3 2 1 ;
3 1 1 ;
6 1 1 : 4 0 1 : 4 2 0 : 4 1 0 ;

Thus, we have the same set and number of collapsed faults based on equivalence fault collapsing.</td></tr>
</table>

Q2.

(i) Iterative Array Model

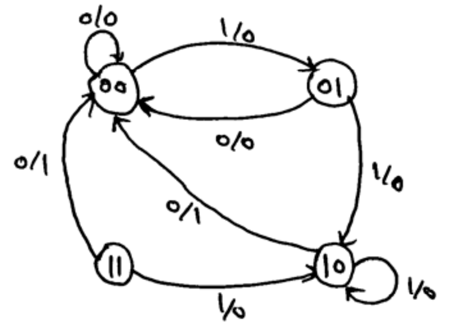


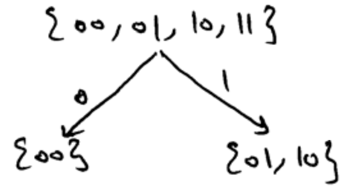
(ii) $D_0 = \bar{q}_0 \bar{q}_1 x$

$D_1 = x (q_0 + q_1)$

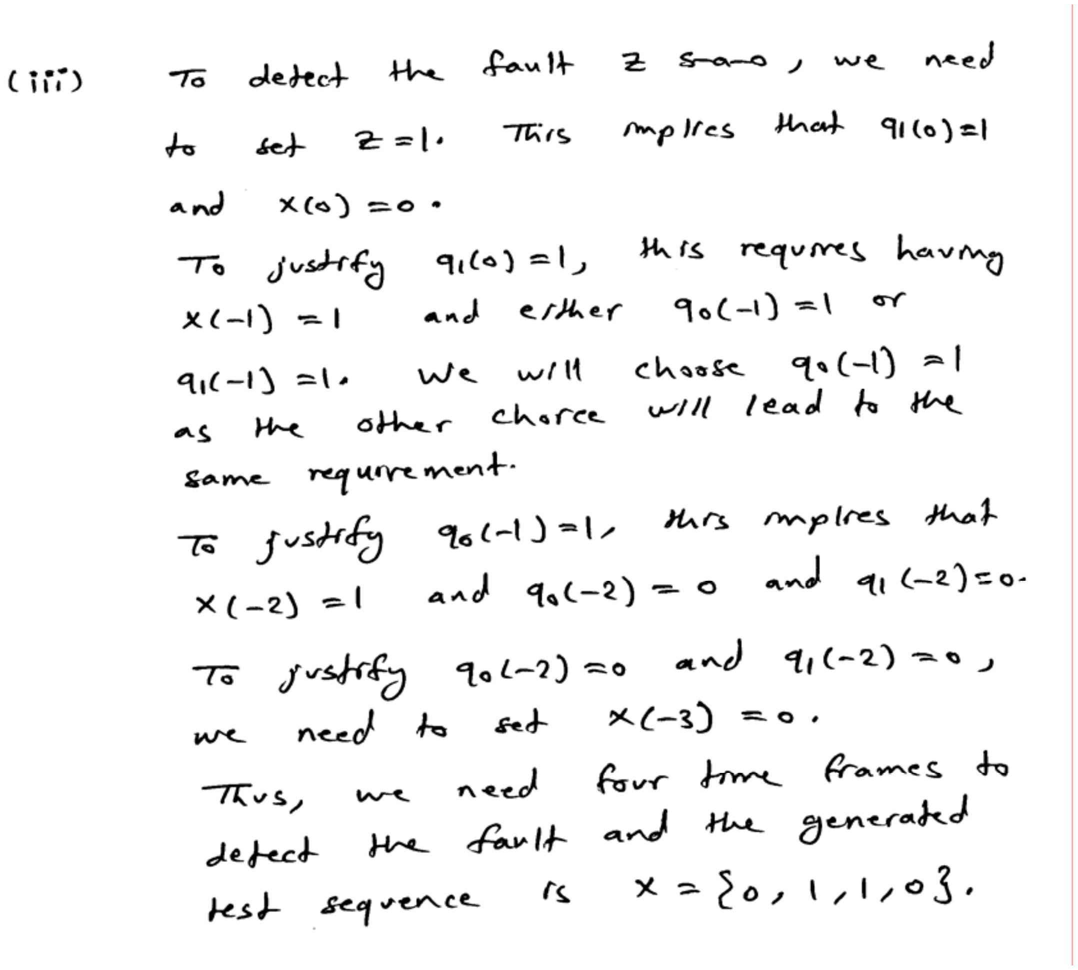
$z = \bar{x} q_1$

State Diagram





Thus, a minimum length synchronizing sequence is x = 0



(iii) To detect the fault z s-a-0, we need to set $z=1$. This implies that $q_1(0)=1$ and $x(0)=0$.

To justify $q_1(0)=1$, this requires having $x(-1)=1$ and either $q_0(-1)=1$ or $q_1(-1)=1$. We will choose $q_0(-1)=1$ as the other choice will lead to the same requirement.

To justify $q_0(-1)=1$, this implies that $x(-2)=1$ and $q_0(-2)=0$ and $q_1(-2)=0$.

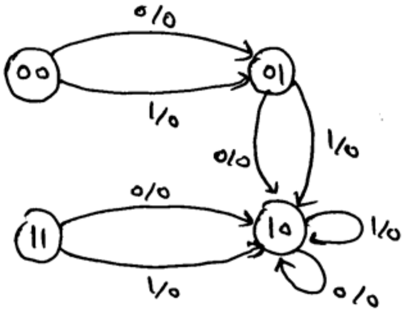
To justify $q_0(-2)=0$ and $q_1(-2)=0$, we need to set $x(-3)=0$.

Thus, we need four time frames to detect the fault and the generated test sequence is $x=\{0,1,1,0\}$.

Verification using PROOFS fault simulator:

Injected Fault	**Signal Names**
11 0 0 : 10 0 0;	1 X 2 Q0 3 Q1 4 G1 5 G2 6 G4 7 G6 8 G3 9 G5 10 Z 11 Z_$OUTPUT
Test Sequence	**Detection Statistics**
1 # This is number of inputs 0 1 1 0 END	0 user time 0.000000 sec sys time 0.016667 sec det faults 1 tot faults 1 coverage 1.000000

(iv) Faulty State Diagram



The faulty machine is synchronizable and can be synchronized with the sequence {0,0} or {0,1}.

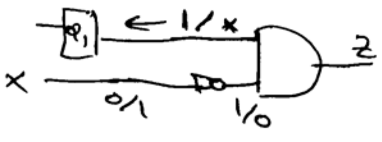
Let us use the initializing sequence I = {0,1} to initialize both the good and faulty machines. The good machine will be initialized to the state 01, while the faulty machine will be initialized to state 10.

A distinguishing sequence between these two states is {1,0} which will produce an output of (0,1) for the good machine and the output (0,0) for the faulty machine. Thus, it is clear that the fault is detectable. Thus, it is also strongly detectable and also partially testable.

The overall test sequence for the fault x s-a-1 is $\{0,1,1,0\}$. To verify this, we show the output response for each of the fault free and faulty states.

	output sequence	
State	Fault Free	Faulty
00	0001	0000
01	0001	0000
10	1001	0000
11	1001	0000

The fault is detectable by HITEC. This is interesting given that the faulty machine is not initializable under 3-valued logic. The fault is detectable because HITEC uses 9-valued logic which will result in requiring only the initialization of the good machine and not the faulty machine. This is because to excite the fault we need to set $x=0$ and to propagate it to the output what we need is a 1 in the good machine but we do not care what value to have in the faulty machine. To get 1 in Q_1 in the good machine we need to apply the sequence $x=\{0,1,1\}$.



Thus, the sequence $\{0,1,1,0\}$ is a test.

Circuit Netlist INPUT(X) OUTPUT(Z) G1 = NOT(Q0) G2 = NOT(Q1) G3 = AND(X, G1, G2) G4 = OR(Q0, Q1) G5 = AND(G4, X) Q0 = DFF(G3) Q1 = DFF(G5) G6 = NOT(X) Z = AND(G6, Q1)	**Signal Names** 1 X 2 Q0 3 Q1 4 G1 5 G2 6 G4 7 G6 8 G3 9 G5 10 Z 11 Z_$OUTPUT
Injected Fault 1 0 1 ;	**Detection Statistics** BACKTRACK LIMIT 10000 STATE BACKTRACK LIMIT 10000 TIME LIMIT 2 system time 0.000 user time 0.000 total faults 1 detected faults 1 redundant finds 0 aborted faults 0 total vectors 4 efficiency 1.0000 coverage 1.0000
Generate Test Sequence 1 # This is number of inputs 0 1 1 0 END	

Thus, we can see that the same test sequence was generated for detecting the fault x stuck-at-1.