

***KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING***

COMPUTER ENGINEERING DEPARTMENT

**COE 545 Digital System Testing
Syllabus - Term 002**

Instructor: Dr. Aiman H. El-Maleh. Room: 22/332 Phone: 2811 Email: aimane

Text Book: *Digital Systems Testing and Testable Design*, by Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman, IEEE Press, 1990.

Course Policies	Assignments	15%
	Project	20%
	Exam I	20%
	Exam II	20%
	Final	25%

Course Topics

1. **Introduction:** The testing problem, costs of testing, test types and schemes.
2. **Fault modeling:** Fault detection and redundancy, fault equivalence, dominance, checkpoints and collapsing. Fault diagnosis. Stuck-at faults, bridging faults, transistor faults, delay faults, etc.
3. **Fault simulation:** serial, parallel, deductive, and concurrent fault simulation. Parallel pattern single fault propagation, critical path tracing and fault sampling.
4. **Test generation for Combinational circuits:** Boolean difference, path sensitization, D-algorithm, PODEM, and FAN. Random test generation, Combined random/deterministic test generation. Test compaction. Cost functions and testability measures.
5. **Test generation for sequential circuits:** Time-frame expansion, extended D-algorithm, BACK algorithm, simulation-based approaches, and complexity of sequential ATPG.
6. **Test generation for CMOS circuits:** Test generation for transistor stuck-open and stuck short faults. Test generation based on gate-level models, robust and non-robust test generation.
7. **Delay-fault testing:** Gate and path delay fault models, robust, validatable nonrobust and nonrobust test vectors, path delay fault simulation and test generation.
8. **Design for testability:** Ad-hoc methods, types of scan cells, LSSD, full scan design, partial scan design, and boundary scan design. Partial scan selection techniques.
9. **Built-in self test:** Theory and operation of LFSR, MISR, random and weighted random pattern testability, BIST pattern generator and response analyzer, scan-based BIST architecture, and test point insertion for improving random testability.
10. **Memory testing:** Functional model, array fault models (stuck-faults, coupling faults and pattern sensitive faults), address decoder fault model, and RAM BIST.
11. **IDDQ testing:** IDDQ detection of defects, IDDQ test patterns, and IDDQ measurement.