COE 545
Digital System Testing
Course Project: Implementation

You are to work on any of the implementation projects given below:

1. **Test Vector Reordering**

   In Order to reduce the time a defective chip spends on a tester until the defect is detected, it is required to order the test patterns in a given test set such that the fault coverage would show the maximum increase with every additional test pattern. This steepens the curve of the fault coverage vs. the number of test patterns. In this project, the student will implement a test vector ordering technique based on the use of Critical Path Tracing. In addition, he will the implement the test vector ordering technique given below and compare with it:

   X. Lin et al. "On Static Compaction and Test Pattern Ordering for Scan Designs", Proc. of Int. Test Set Conference, 2001, pp. 1088 1097.

2. **Test Data Compression**

   In order to reduce the test data volume and reduce the test cost, the use of efficient test data compaction and compression techniques is imperative. In this project, the student will investigate and implement a new test data compression technique based on coding theory.

3. **Test Compaction for Sequential Circuits based on reverse order test vector restoration**

   A very efficient Test sequence compaction technique for sequential circuits was proposed recently based on reverse order test restoration. In this project, the student will implement this technique. The technique is based on the paper shown below:

   R. Guo et al, "Reverse-Order-Restoration-Based Static Test Compaction for Synchronous Sequential Circuits", IEEE Trans. CAD, 2003, pp. 293-304.

4. **State Encoding for low power and testability based on Genetic algorithms**

   In this project, the student will implement a state assignment algorithm targeting both low power and high testability based on Genetic algorithm. Comparison will be made with the paper below:

   G. Venkataraman et al. "GALLOP: Genetic Algorithm Based Low Power FSM Synthesis by Simultaneous Partitioning and State Assignment", Int. Conf. VLSI Design, 2003.

5. **Improving the performance of Test Set Relaxation for combinational circuits.**

   Recently, a very efficient test relaxation technique for combinational circuits has been proposed. In this project, the student will implement some ideas aiming at increasing the percentage of extracted X's. The work is based on the paper given below:

   Aiman El-Maleh *and Ali Al-Suwaiyan, "An Efficient Test Relaxation Technique for Combinational and Full-Scan Sequential Circuits" Proc. of the 20'th* ***IEEE VLSI Test Symposium (VTS)****, pp. 53-59, 2002.*

6. **Improving the performance of critical path tracing**

   Critical Path Tracing is a very efficient algorithm for fault simulation that can be as fast as fault simulation techniques based on concurrent faut simulation. The advantage of CPT algorithm that it can fault simulate a test set witoout fault dropping at the same cost of fault dropping. This is significant for test compaction algorithms that require fault simulation without dropping. In this project the student will implement techniques to improve the performance of an existing CPT implementation. It is based on ideas from the paper given below:

   M. Abramovici et al., "Critical Path Tracing: An Alternative to Fault Simulation," IEEE Design & Test of Computer, Vol. 1, No. 1, pp. 83-93, Feb. 1984.