June 10, 2003

COMPUTER ENGINEERING DEPARTMENT

COE 545

Digital System Testing

Final Examination

Second Semester 2003 (022)

Time: 7:00-9:30 PM

Student Name : _____

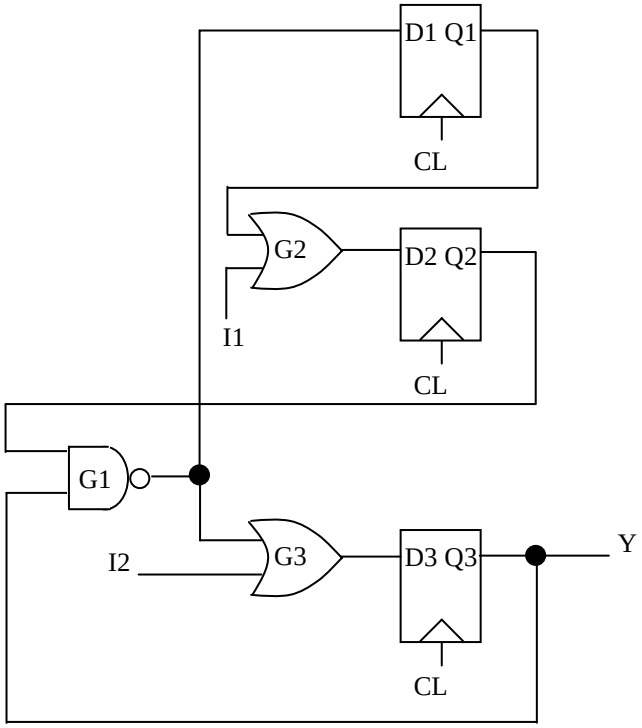
Student ID. : _____

Question	Max Points	Score
I	30	
II	15	
III	15	
IV	15	
V	25	
Total	100	

Dr. Aiman El-Maleh

[30 Points]

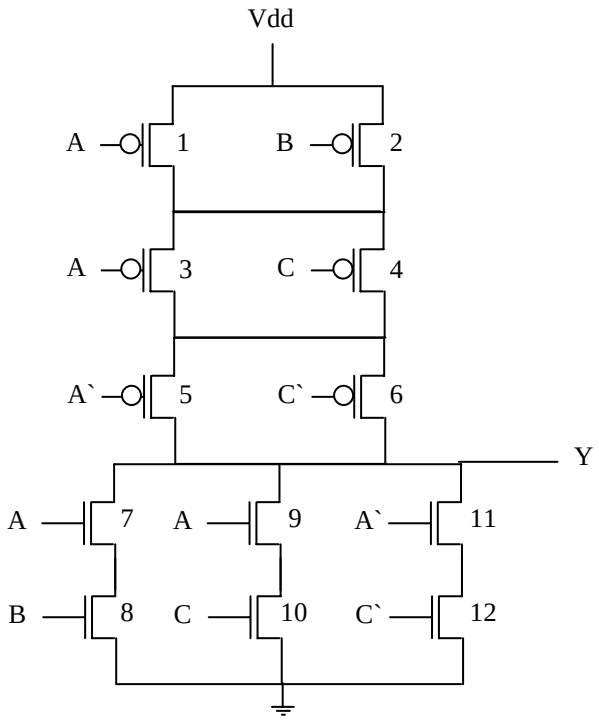
(I) Consider the sequential circuit shown below, where the sequential elements are D-FFs, I1 and I2 are primary inputs and Y is a primary output:



1. Determine the FFs that have to be scanned to make the circuit balanced. Then, determine the appropriate scan FF to be used and show the partial-scanned circuit. Furthermore, explain how the fault G2 stuck-at-1 can be detected by the balanced partial-scanned circuit.
2. Convert the circuit into a full-scanned circuit using multiplexed data FF. Then, explain how the fault G2 stuck-at-1 can be detected by the full-scanned circuit.
3. Assume that to enhance the testability of the circuit, it is required to add an observation point on the D input of FF1, a 0-injection control point on the output of G2, and both a 0 and 1 injection on the output of G1. Modify the design so that it has the desired features such that the control and observation points are driven by a scan register. Assume that during the scan operation, the normal state of the circuit should not be disturbed.

[15 points]

(II) Considering the CMOS circuit shown below, generate robust tests to detect the indicated transistor stuck-open (TSOP) faults. Furthermore, generate a test for the indicated transistor stuck-short (TSST) fault and determine the conditions necessary for its detection.

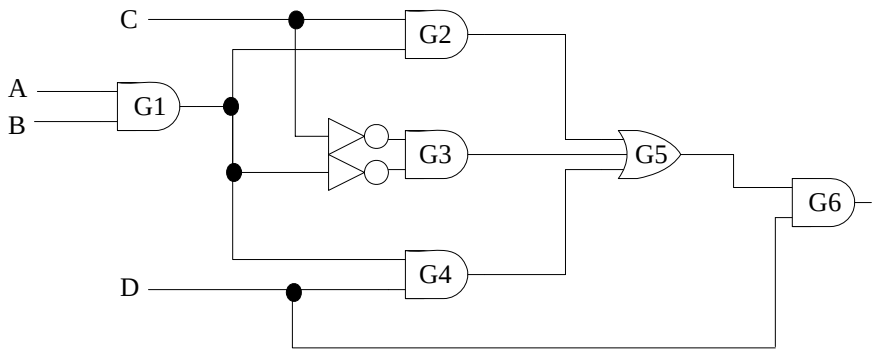


1. P1 TSST.
2. N7 TSOP.
3. The multiple fault N7 TSOP and P4 TSOP.

[15 points]

(III) Considering the circuit shown below, determine whether each of the indicated path delay faults is robust testable, validatable non-robust testable, non-robust testable, or untestable. Justify your answer.

1. The output falling transition along the path {A, G1, G2, G5, G6}.
2. The output rising transition along the path {A, G1, G2, G5, G6}.
3. The output rising transition along the path {A, G1, G4, G5, G6}.



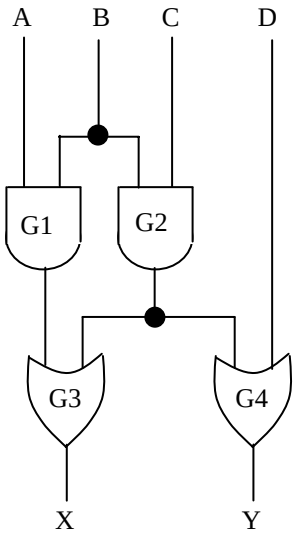
[15 points]

(IV) Determine the minimum number of clock cycles required to test each of the following designs. Justify your answer.

1. A double-latch LSSD design with 20 SRLs and 50 test vectors.
2. A LSSD single-latch design using conventional SRLs where n=4 and m=8. Assume that N1 requires 20 test vectors and N2 requires only 10.

[25 points]

(V) Consider the following Combinational circuit with four PIs and two POs. Assume that the output of G2 is stuck-at-0. Furthermore, assume that type 1 LFSR is used in the implementation of the random test generator with a characteristic polynomial $p(x)=1+x+x^4$ while type 2 LFSR is used in the implementation of the test response analyzer with a characteristic polynomial $p(x)=1+x+x^2$.



1. Show the complete circuitry required to test the given circuit using the built-in evaluation and self-test BIST architecture. Determine the fault-free and faulty signatures and indicate if the fault will be detected after four clock cycles. Assume that the random test generator is seeded with the value 0001 and the test response analyzer with the value 00.
2. Show the complete circuitry required to test the given circuit using the LSSD on-chip self-test BIST architecture. Assume that the random test generator is seeded with the value 0110 and the test response analyzer with the value 00. Identify the fault-free and faulty signatures after applying the first test vector and determine whether the fault is detected or not. Assume that the scan chain is loaded initially before applying BIST with all 0's.