KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 464 Testing of Digital Circuits (3-0-3)
Syllabus - Term 042

Catalog Description

Introduction to the testing problem, fault modeling, e.g., stuck-at, bridging, transistor-open and transistor-short faults. Fault simulation, gate-level testing, automatic test pattern generation (ATPG) algorithms. Testing of regular structures. Testing of sequential circuits. Signature analysis. Design-for-testability (DFT).

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Office Hours SMW 11:00-12:00 PM (and by appointment)

Text Book: *Digital Systems Testing and Testable Design, by Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman, IEEE Press, 1990.*

Course Policies

Assignments	15%
Quizzes	15%
Project	20%
Midterm	20%
Final	30%

- Assignments are to be submitted in class in the specified due date.
- Late assignments will be accepted but will be penalized 10% per each late day.

Course Topics

1. ***Introduction:*** The testing problem, costs of testing, test types and schemes.
2. ***Fault modeling***: Fault detection and redundancy, fault equivalence, dominance, checkpoints and collapsing. Fault diagnosis. Stuck-at faults, bridging faults, transistor faults, delay faults, etc.
3. ***Fault simulation:*** serial, parallel, deductive, and concurrent fault simulation. Parallel pattern single fault propagation, critical path tracing and fault sampling.
4. ***Test generation for Combinational circuits:*** Boolean difference, path sensitization, D-algorithm, PODEM, and FAN. Random test generation, Combined random/deterministic test generation. Test compaction. Cost functions and testability measures.
5. ***Test generation for sequential circuits***: Time-frame expansion, extended D-algorithm, BACK algorithm, simulation-based approaches, and complexity of sequential ATPG.

6. ***Test generation for CMOS circuits:*** Test generation for transistor stuck-open and stuck short faults. Test generation based on gate-level models, robust and non-robust test generation.
7. ***Delay-fault testing***: Gate and path delay fault models, robust, validatable nonrobust and nonrobust test vectors.
8. ***Design for testability***: Ad-hoc methods, types of scan cells, LSSD, full scan design, partial scan design, and boundary scan design. Partial scan selection techniques.
9. ***Built-in self test***: Theory and operation of LFSR, MISR, random and weighted random pattern testability, BIST pattern generator and response analyzer, scan-based BIST architecture, and test point insertion for improving random testability.