

Name: Key

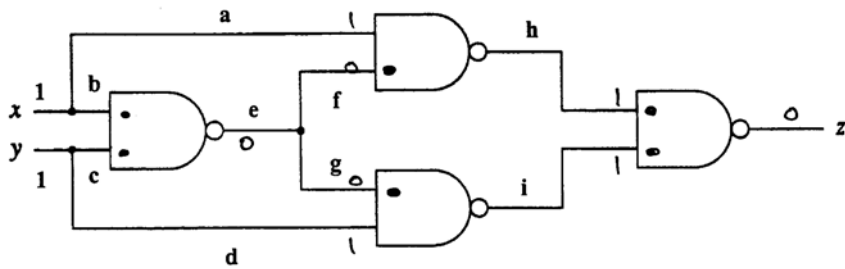
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COE 464, Term 042
Testing of Digital Circuits

Quiz# 4

Date: Tuesday, March 29, 2005

Q1. Consider the circuit given below and assume that you have all the single stuck-at faults in the circuit, without fault collapsing, to be fault simulated under the test vector $xy = \{11\}$:



- i. Logic simulate the circuit and mark the sensitive inputs of each gate with a •.
- ii. Using **Critical Path Tracing** technique, determine the set of faults detected by the test vector $xy = \{11\}$. Write your solution in the table given below.

FFR Traced	Critical Lines	Stems to check	Stem Checked	Capture Line
z	z, h, i, f, g	e	e	z
e	e, b, c	x, y	x	i or z
x	x	y	y	h or z
y	y	∅		

Set of faults detected is: z1, ho, io, fi, gi, e1, bo, co, xo, yo