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Presentation of

"Diagnosing combinational Logic Design using SLAT Paradigm"

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Introduction

A new way of diagnosing ICs that fail logic tests will be technique of discussed. It can handle bridging fault, opens, transition faults and many more complex defects as easily and as accurately as regular stuck-at faults.

Standard Techniques – General approach

- Collecting set of defects.
- Translation of defects into logic faults by using fault simulators
- Comparing simulated results against data collected at test site
- Disadvantage: Single stuck-at Faults model will diagnose most faults but not all.

Diagnostic Techniques

Standard Techniques - Recent Technique

- Does not require logic modeling
- No effect cause analysis
- Has 3 Basic Ideas
  - ✓ Focus on defect location
  - ✓ Diagnostic success does not mean full explanation
  - ✓ Diagnostic fail tests are not independent entities

Diagnostic Techniques

SLAT Diagnostic Approach

- Combination of pins as logical defects
- Reduced complex diagnostic output
- Associated with an assumption
- SLAT property attached with Failing Pattern
- 3 types of patterns
  - SLAT Pattern
  - Failing Pattern
  - Non-failing pattern

It consists of three phases:

- Phase I: SLAT Patterns Identification
- Phase II: Finding explaining Multiplet
- Phase III: Splat formation

SLAT-based diagnosis

- **Initial Diagnosis**
  - Patterns identification
  - Consist of loop over failing patterns
  - Flow chart approach
  - Table creation for describing relationship between SLAT patterns and pins that explain those patterns.

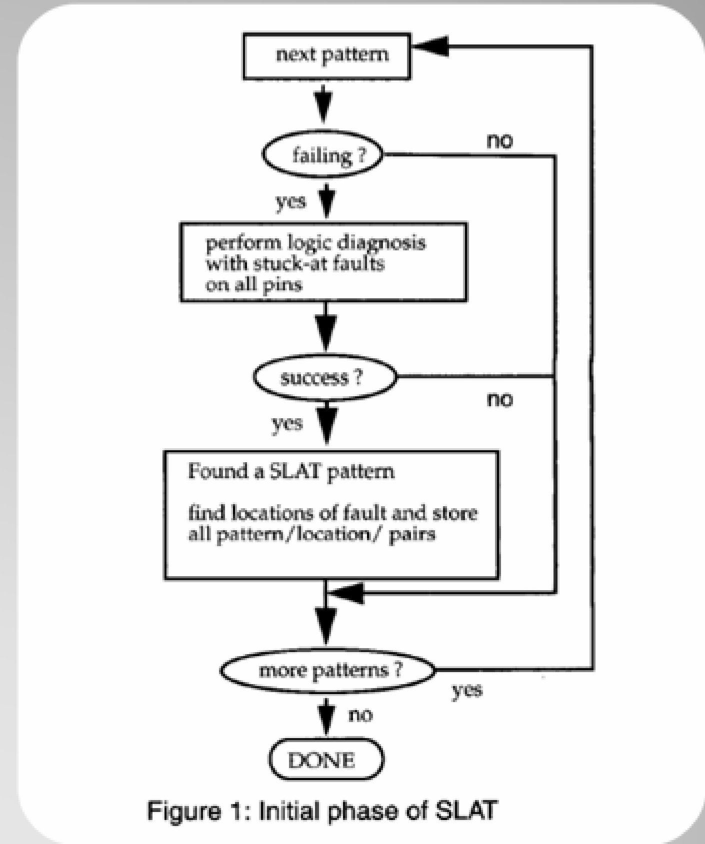

Figure 1: Initial phase of SLAT

Phase One: SLAT Patterns Identification

Phase II: Finding explaining Multiplet

- Finding sets of pins such that each SLAT pattern is explained by at least one pin in the set.
- The minimal sets are called Multiplets.

```
Struct DefectList  * Dlist;
LocalMaxDefectSize = MaxDefectSize
Dlist = FindDefects ();

struct DefectList  * FindDefects () {
  struct DefectList  * Dptr = (struct DefectList *)NULL;
  struct DefectList  * foundDptr;

   // Find target_pattern, the pattern that has not yet been flagged
   // as explained, and that, among the unexplained patterns, has
   // the smallest number of explaining pins.
   // If there are no unexplained patterns left,
   // return pointer to an empty defect list.

   if (!Find_target_pattern()) return empty defect_list

   if (!LocalMaxDefectSize) return NULL pointer

   // Look for more unexplained patterns
   LocalMaxDefectSize--;
   Loop over all pins that explain target_pattern {
     Increase the explain counts of all the patterns
       explained by this pin.
     if (foundDptr = FindDefects()) {
       Add pin to all the defects in the list pointed at
         by foundDptr
       if (!Dptr) Dptr = GetCumulativeDefectList()
       Merge the list pointed at by foundDptr into
         the cumulative defect list pointed at by Dptr
     }
     Decrease the explain counts of all the patterns
       explained by this pin
   }
   LocalMaxDefectSize++;

   return (Dptr);

   }
```

Figure 2: Program fragment to find multiplets

```
37 SLAT patterns were found.
The returned multiplet size is 3.
40 multiplets were found.

Multiplet 1:
 pin index 1.
 pattern 1        fault 1 ISA1
 Pattern 2        fault 1 ISA1
   .
   .
 pin index 3.
 pattern 10       fault 2 OSA1
 pattern 11       fault 2 OSA1
   .
   .
 pin index 7.
 pattern 80       fault 3 ISA1
 pattern 81       fault 3 ISA1
   .
   .

Multiplet 2:
 .
 .
```

Figure 3: Example of SLAT diagnosis output (partial

Phase III: Splat formation

- Define sets called Splat.
- Splat is a set of one or more pins such that each pin in the set belongs to some multiplets
- No two pins in the same splat belong to same multiplet.

19 patterns failed but were not SLAT patterns.
37 SLAT patterns were found.
The returned multiplet size is 3.
40 multiplets were found.

The 2 pins in splat 1 are:
pin index 1
pin index 2

The 4 pins in splat 2 are:
pin index 3
pin index 4
pin index 5
pin index 6

The 5 pins in splat 3 are:
pin index 7
pin index 8
pin index 9
pin index 10
pin index 11

Figure 4: SLAT output for a complete set of multiplets

- The actual pins that can be effected by the defect are localized within its particular splat.

Interpretation

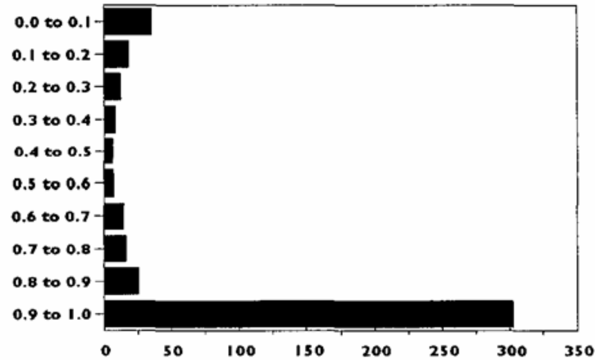

Figure 5: Distribution of the ratios of SLAT patterns to failing patterns

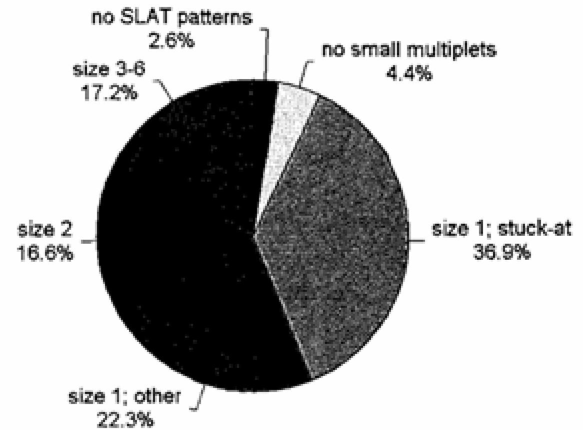

Figure 6: Experimental SLAT diagnostic results.

experimental

In this paper, author have discussed a new way of diagnosing ICs that fail logic test. SLAT uses a new defect model as the engine for its diagnosis that defines a logical defects as the minimal set of pins that can be affected by the physical defect.

conclusion