Title of Paper
“Dominance based analysis for large volume production fail diagnosis”

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Abstract

- In this paper, a procedure for using fault dominance in a large volume diagnosis environment is described.
- Fault dominance is shown to be useful for reducing the fault simulation time during fault diagnosis when used together with the concept of pattern dependence and maximally dominating faults.
- Results for both ISCAS benchmarks and industrial circuits are reported.
- The results show 9% to 44% average reduction in the fault simulation time for these circuits.

Introduction

- Fault diagnosis and physical failure analysis aid in locating the root cause of failures, which can improve the yield significantly.
- Since fault diagnosis can be time consuming, improving the speed of diagnosis is very important in enabling large volume diagnosis.
- Different methods to reduce ATPG and fault diagnosis time by reducing the fault list size have been proposed.
- Two of these fault collapsing concepts are based on:
  - equivalent fault identification
  - dominant fault identification.

Fault Dominance

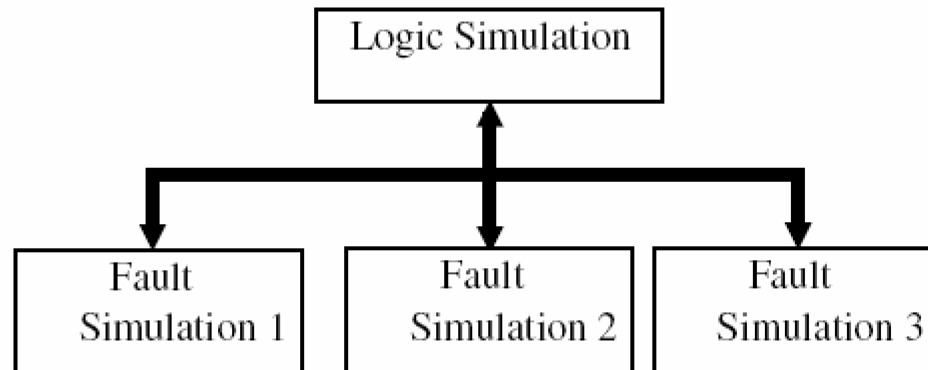
- A fault f1 dominates a fault f2 under a test set T, if for every test Ti in T that detects f2 on a set of outputs Z, f1 is also detected by Ti on the set of outputs Z.
- Hence, if f1 is not detected by a test, it implies that f2 will not be detected by the test.
- This property allows fault simulation for f2 to be avoided for a test that does not detect f1, reducing the fault simulation time during fault diagnosis.
- This observation is used in this paper to speed up diagnosis procedure.

Components of dominance based diagnosis

- Dominance based diagnosis is a multiphase diagnosis process, where a subset of faults is considered in the first phase.
- Based on the results of fault simulation for this subset, additional faults are then simulated in a second phase.
- In the implementation, phases 1 and 2 are alternated for every test pattern.
- This allows to store the results of logic simulation for every test pattern when it is considered, which alleviates the need to recompute fault free values.

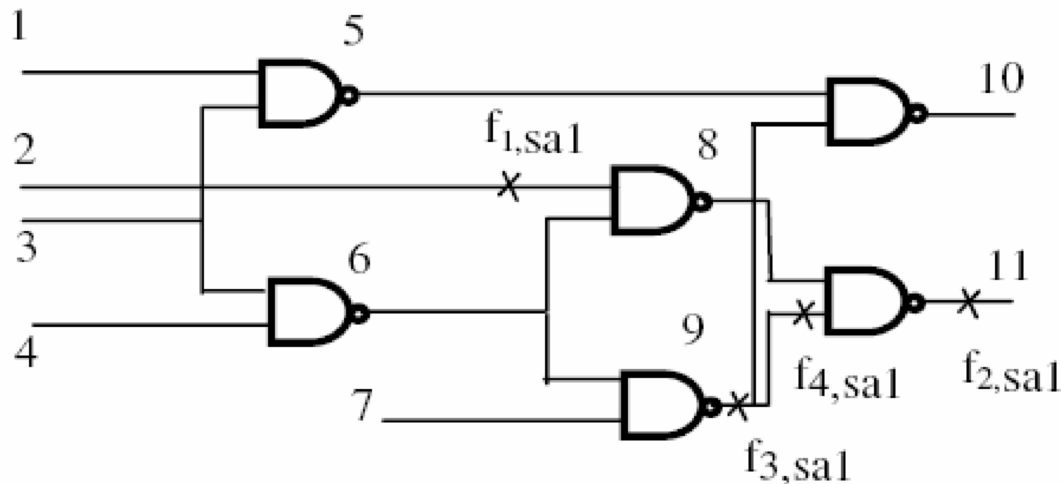
Components of dominance based diagnosis

- To further reduce the contribution of logic simulation time to the overall diagnosis time, especially when a large volume of failing die is to be diagnosed, it is possible to exploit parallelism existing among the different diagnosis runs.
- In this approach, the cost of logic simulating a test pattern can be amortized over large numbers of diagnosis cases.



Dominance relations (Rule 1)

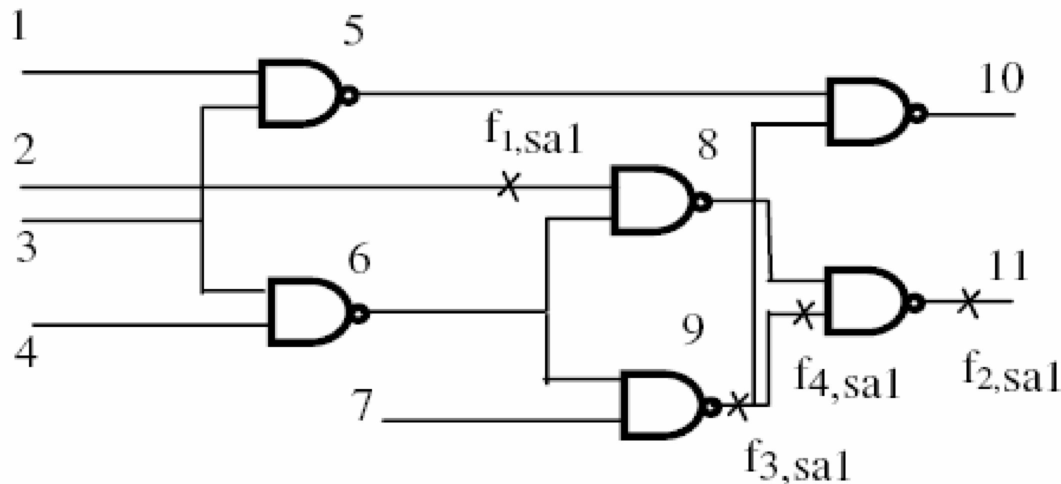
- Consider two faults f1 and f2 on outputs of gates g1 and g2, where f1 is g1 stuck-at a1, f2 is g2 stuck-at a2, and a1,a2 є {0,1}.
- Suppose that there is at least one combinational structural circuit path between f1and f2.
- Suppose that g1 and g2 are in the same fanout free region of the circuit and g1 drives g2.
- If the number of inversions between g1 and g2 is even, then a1=a2 otherwise a1=a2'.
- Under these conditions, every test that detects g1 stuck-at a1 also detects g2 stuck-at a2. Hence, f2 dominates f1.



f2 dominates f1

Dominance relations (Rule 2)

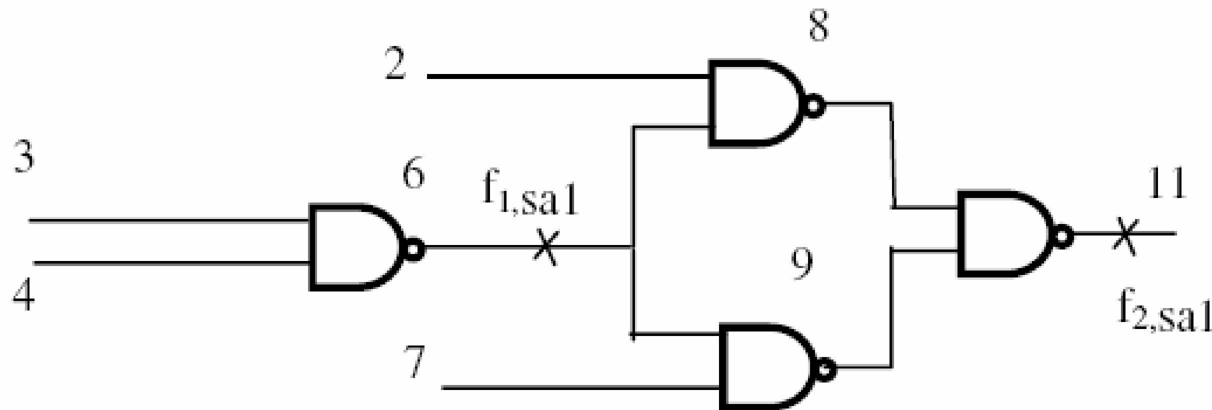
- If g2 is a fanout stem, g1 is one of the fanout branches and a1 = a2, then any test for f1 will detect f2 as long as the fault effect of f2 is not masked through a path from one of the other fanout branches.
- Masking can occur if there exists a path from g2 that reconverges with the propagation path for fault f1 and the paths have opposite numbers of inversions between g2 and the point of reconvergence. If masking cannot occur then f2 dominates f1.



f3 dominates f4

Dominance relations (Rule 3)

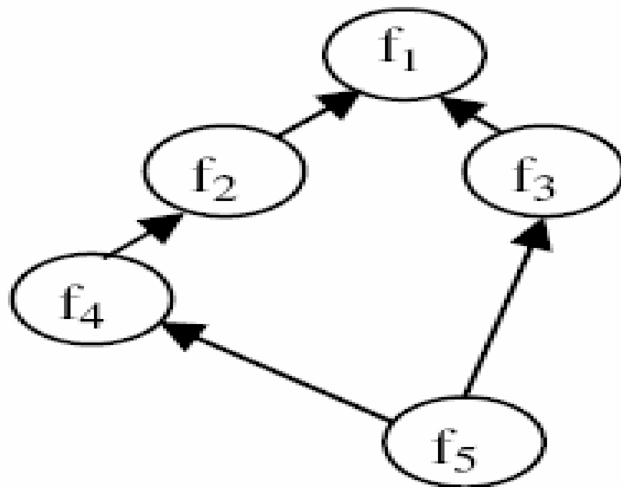
- Suppose that g1 is a fanout stem and g2 is the output of the gate at which all the paths from g1 reconverge.
- Suppose in addition that all the paths from g1 to g2 have the same polarity.
- If the number of inversions between g1 and g2 is even, then a1=a2, otherwise a1=a2'.
- Under these conditions, any test, which detects g1 stuck-at a1, also detects g2 stuck-at a2. Hence, f2 dominates f1.



f2 dominates f1

Dominance Graph

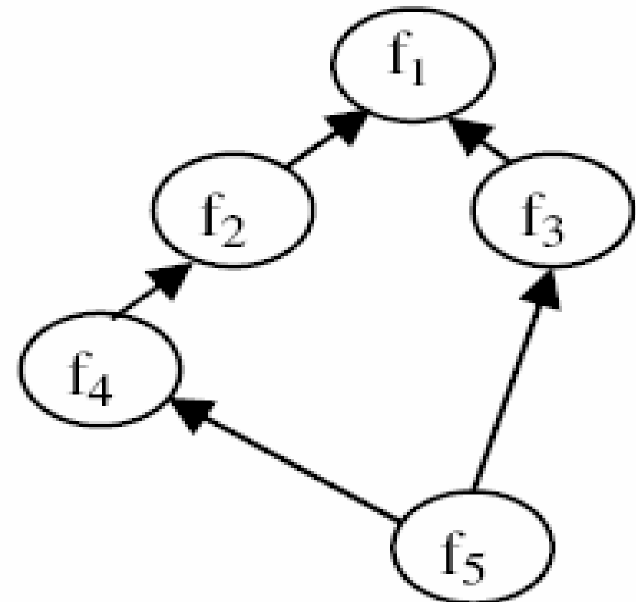
- The dominance relations can be represented in the form of a directed graph called the dominance graph.
- In the graph, the vertices represent the faults fi, fj etc.
- A directed edge from fault fi to fj indicates that fj dominates fi.



f1 dominates f2
f1 dominates f3
By transitivity,
f1 dominates f4,f5

Maximally dominating faults

- A fault is called a maximally dominating fault, if it is not dominated by any other fault.
- **Level of a fault fi: Level(fi)** is defined as the length (in nodes) of the shortest path between fi and a maximally dominating fault.
  - fault f1 has Level(f1) =1,
  - fault f2 has Level(f2) = 2
  - fault f5 has Level(f5) = 3.



Pattern Dependence

- A fault f_p is a pattern dependent version of a conventional (pattern independent) fault f if f_p may not cause faulty values at all the outputs and for all the tests where f produces faulty values.
- A faulty response R2 is a pattern dependent version of a faulty response R1, if R1 has all the faulty values observed in R2. R1 may also have faulty values at more observation points than R2.
- If a fault f1 dominates another fault f2, then for a test set T, the response R2 of fault f2 is a pattern dependent version of the response R1 of fault f1.
- Only if f1 is detected at a set of outputs Z,

  f2 can be detected at a subset of the outputs Z.

	R_1	R_2
T1	101	100
T2	011	001
T3	001	001

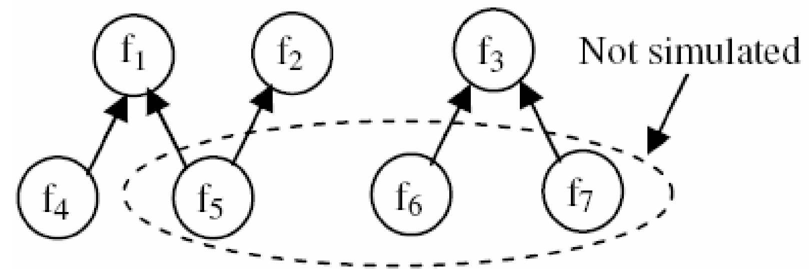
R2 is a pattern-dependent version of R1

Conditional Pruning of Dominance Graph

- By pruning out dominated faults using the concepts of maximally dominating faults and pattern dependence, a significant reduction in the number of faults simulated during diagnosis is possible.

Conditional Pruning of Dominance Graph (Example)

- Response R is a pattern-dependent version of R1 but not of R2 and R3.
- Since the maximally dominating faults f2 and f3 do not explain the observed response R, the faults dominated by f2 and f3 can also be pruned out, since they will also not explain the response R.
- At the next phase, since f5, f6 and f7 are pruned out, only fault f4 needs to be simulated as it may explain the defect in the circuit.



(a) Dominance graph

R	$R_1(f_1)$	$R_2(f_2)$	$R_3(f_3)$
001	011	100	110

(b) CUT and fault response

Dominance based diagnosis procedure

- The concepts of fault dominance and pattern dependence are integrated with an effect-cause diagnosis procedure.
- When dominance is used, fault simulation proceeds in a stepwise manner.
- Initially, all the faults at level one of the dominance graph (the maximally dominating faults) are simulated.
- At each following step, the faults at the immediately lower levels are simulated or pruned, conditionally based on the response of their dominating faults.
- This conditional pruning and simulation of the subtrees of the dominance graph at each level can result in significant reduction in the fault simulation time.

Dominance based diagnosis procedure

1. Read dominance graph
2. For each failing test pattern
   i. Logic simulation
   ii. For each level j of dominance graph, where j =1,2,..
      1. Fault simulation: Level j.
      2. Prune dominance graph subtrees of level j.
      3. New fault list : Faults F_{j+1} at level j+1
      4. If (F_{j+1} = = ϕ), break to next test pattern.

      End

   End

Experiments and Results

- Full scan versions of three large ISCAS'89 benchmarks and four large industrial circuits called C1 to C4 are used.
- Some characteristics of these circuits are given below.

Circuit	Gates	Faults	Numfail	Maxdom(%)
S13207	7K	9.7K	233	22.33
S15850	9K	11K	191	24.77
S38417	22K	31K	350	26.66
C_1	117K	170K	759	32.32
C_2	444K	637K	794	34.27
C_3	526K	938K	567	30.24
C_4	1337K	3714K	26	38.73

Experiments and Results

- 100 random stuck-at-faults are injected and diagnosis is performed for each fault.
- The effect of dominance on fault simulation time during diagnosis is shown below.

Circuit	N_{nodom}	N_{dom}	$E_{impr}(\%)$	$T_{nodom}(s)$	$T_{dom}(s)$	$A_{impr}(\%)$	$B_{impr}(\%)$	$W_{impr}(\%)$
S13207	1063823	300043	71.79	2.32	1.31	43.54	80.00	14.28
S15850	857652	303638	64.59	3.12	1.84	41.02	57.69	6.97
S38417	1180867	477832	59.53	2.75	1.81	34.18	68.42	0.50
C_1	1480694	625432	57.76	16.06	11.28	29.76	52.48	7.77
C_2	1201881	710689	40.86	110.56	99.71	9.81	24.07	0.30
C_3	11584723	6114766	47.21	195.89	172.59	11.89	26.46	0.42
C_4	483783	274937	43.16	39.56	28.57	27.78	65.21	0.00

Conclusion

- Fault dominance was used in a diagnosis procedure to trade off a small amount of preprocessing time to avoid a large amount of fault simulation time.
- The reduction in the fault simulation time is a function of the number of maximally dominating faults and the number of dominance relations.
- The smaller the number of maximally dominating faults, the greater the reduction in the fault simulation time.
- Experimental results show 9-44% reduction in the fault simulation time for ISCAS benchmarks and industrial circuits.
- Reducing the set of maximally dominating faults by additional analysis can further speed up dominance based diagnosis.

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