COE 571 Digital System Testing

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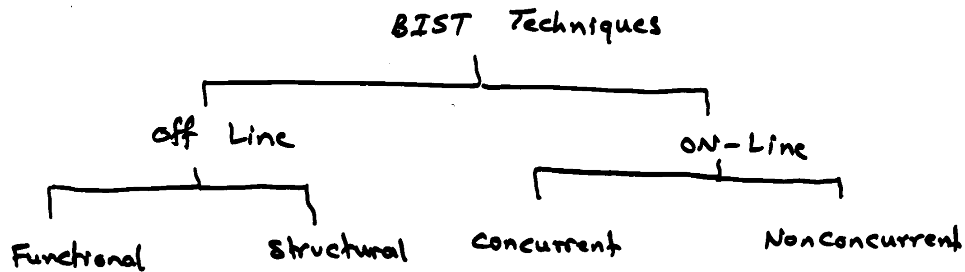
Built In Self Test (BIST)

1. **Generic BIST architectures**
2. **Centralized & separate board-level BIST architecture (CSBL)**
3. **Built-in evaluation and self test (BEST)**
4. **Random test socket (RTS)**
5. **LSSD on chip self test (LOCST)**
6. **Self testing using MISR and parallel SRSG (STUMPS)**
7. **Concurrent BIST (CBIST)**
8. **Multiple input signature register (MISR)**
9. **Centralized and embedded architecture with boundary scan (CEBS)**
10. **Random test data BIST architecture (RTD)**
11. **Simultaneous self test (SST)**

Built-In Self Test (BIST)

- BIST is the capability of a circuit (chip, board, or system) to test itself.

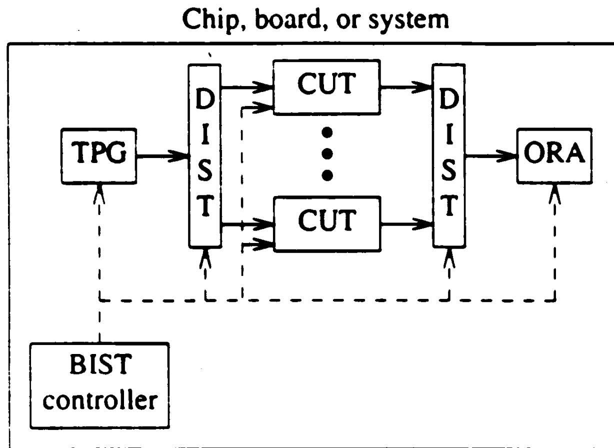


- Off-line BIST architectures can be classified:
  1. Centralized or distributed BIST circuitry
  2. Embedded or separate BIST elements

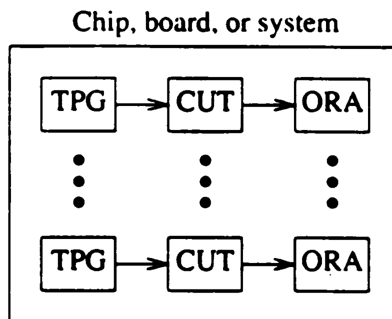
- BIST architectures consist of several key elements:
  1. Test pattern generators
  2. Output-response analyzers
  3. Circuit under test (CUT)
  4. Distribution system for transmitting data from TPGs to CUTs and from CUTs to ORAs
  5. BIST controller for controlling BIST circuitry and CUT during self-test.

Generic BIST Architectures

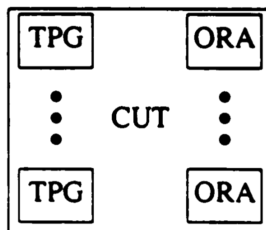
- centralized and separate BIST architecture



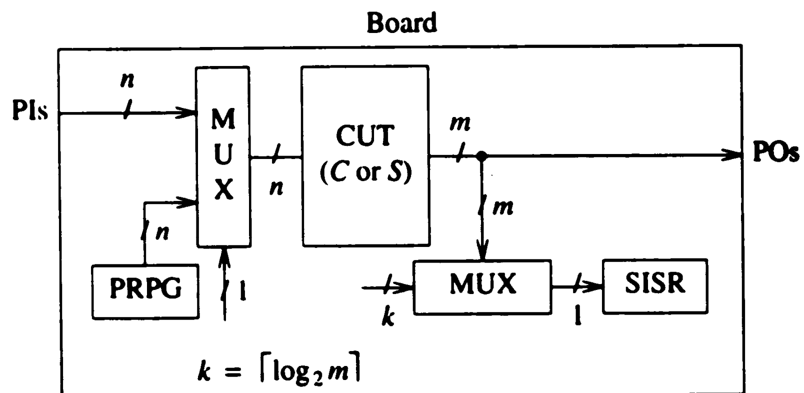
- distributed and separate BIST architecture



- distributed and embedded BIST architecture



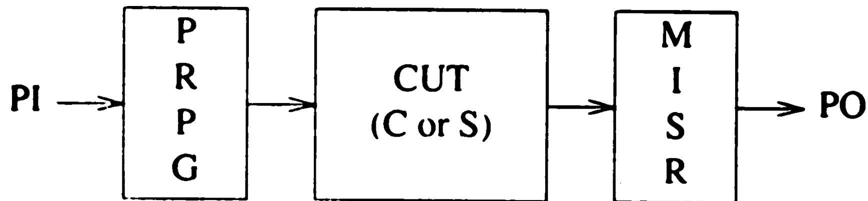
Centralized & Separate Board-Level BIST Architecture (CSBL)



- Inputs are driven by a PRPG
- Outputs monitored by single-input signature analyzer
- Test is repeated m times, once for each output
- Extensive fault simulation is required to determine # vectors to achieve adequate fault coverage.

Built-In Evaluation and Self-Test (BEST)

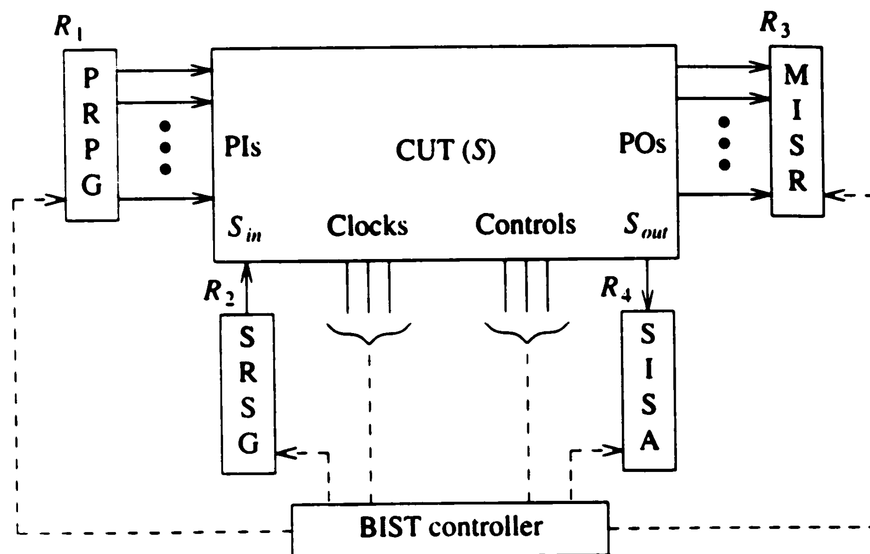
- In general, CUT is sequential circuit



- Inputs are driven by PRPG
- outputs are compressed using MISR
- Both an embedded and separate version of architecture exist
- For some circuits, this method ineffective in acheiving acceptable fault coverage
- Low hardware overhead

Random - Test Socket (RTS)

- Assumes Full-Scan - Test per scan

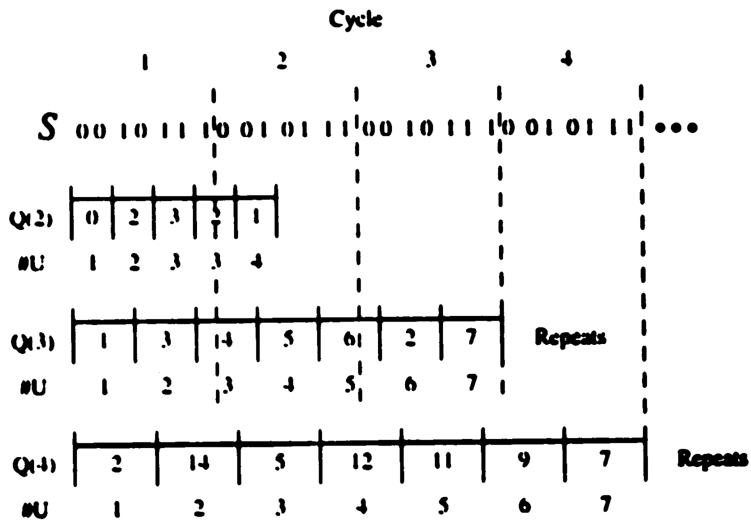


- Testing process:

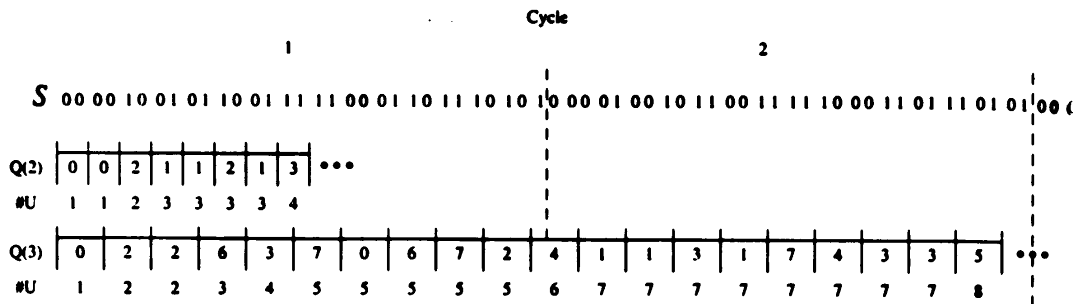
1. Initialize the LFSRs
2. Load a pseudorandom test pattern into scan path using R2
3. Generate a new pseudorandom test pattern using R1 (applied to PIs)
4. Capture response on POs on R3
5. Execute a parallel-load operation on system storage cells to capture response
6. Scan out data in the internal scan path and compress it in R4.
7. Repeat steps 2-6

Test Patterns Generated by LFSRs

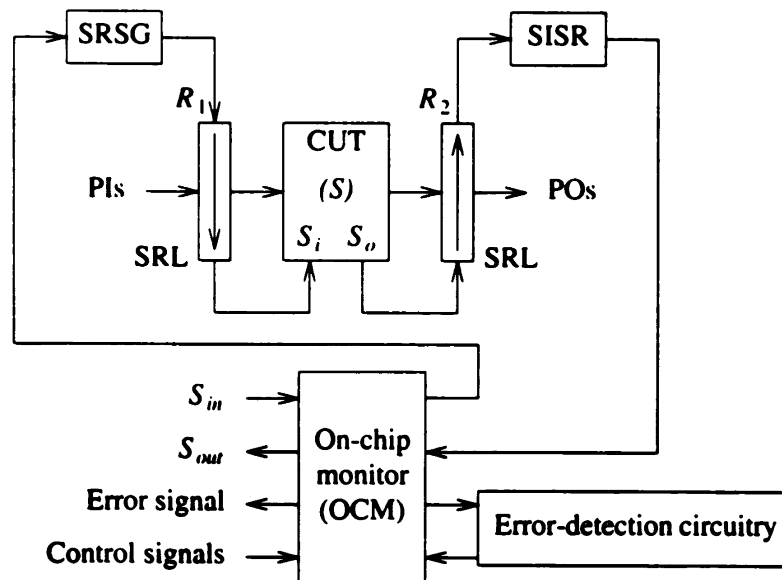
$P(x) = 1 + x^2 + x^3$; seed = 100



$P(x) = 1 + x^3 + x^5$; seed = 10000



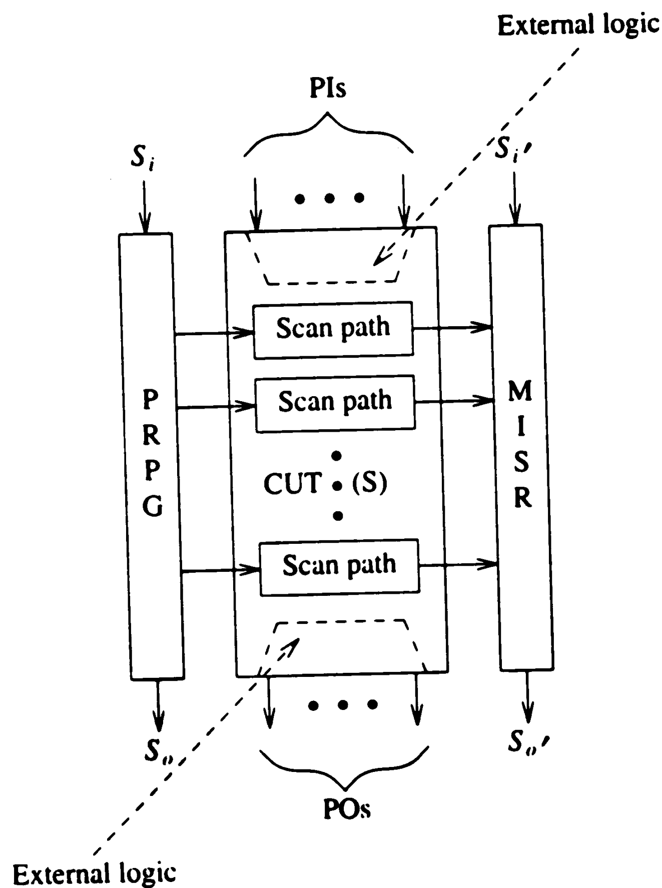
LSSD On-chip Self-Test (LOCST)



Test Process:

1. Initialize: load scan path with seed data
2. Activate self-test mode: disable system clocks on R1 & R2; enable LFSR operation
3. Execute self-test operation:
   a. Load scan path with pseudorandom test. Data in scan path is compressed in SISR.
   b. Activate system clock for one cycle; R2 & internal scan path will capture system data
   c. repeat a & b
4. Check result: compare final value in SISR with known good signature.

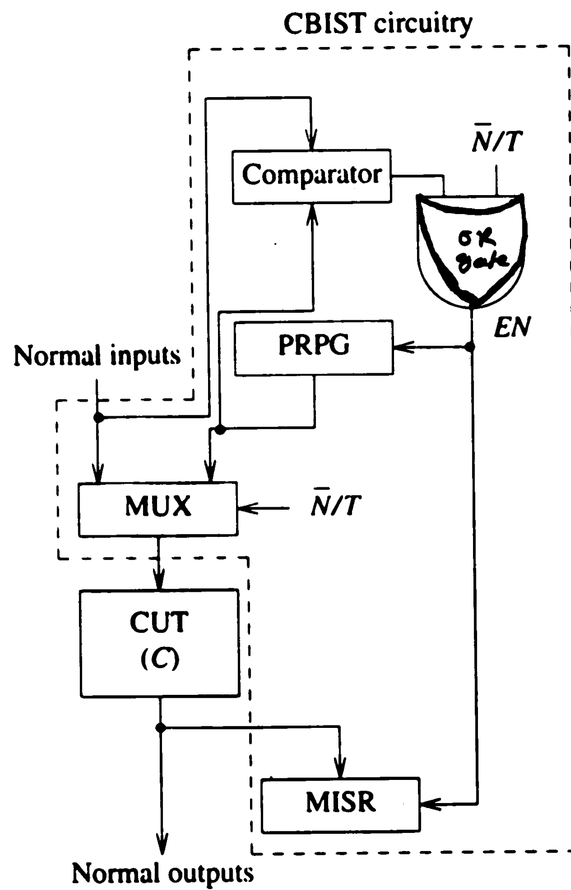
Self-Testing using MISR and Parallel SRSG (STUMPS)



- Scan paths driven in parallel by PRPG
- Signature generated in parallel from each scan path using a MISR
- Significant reduction in test time
- Problem with correlation of test data

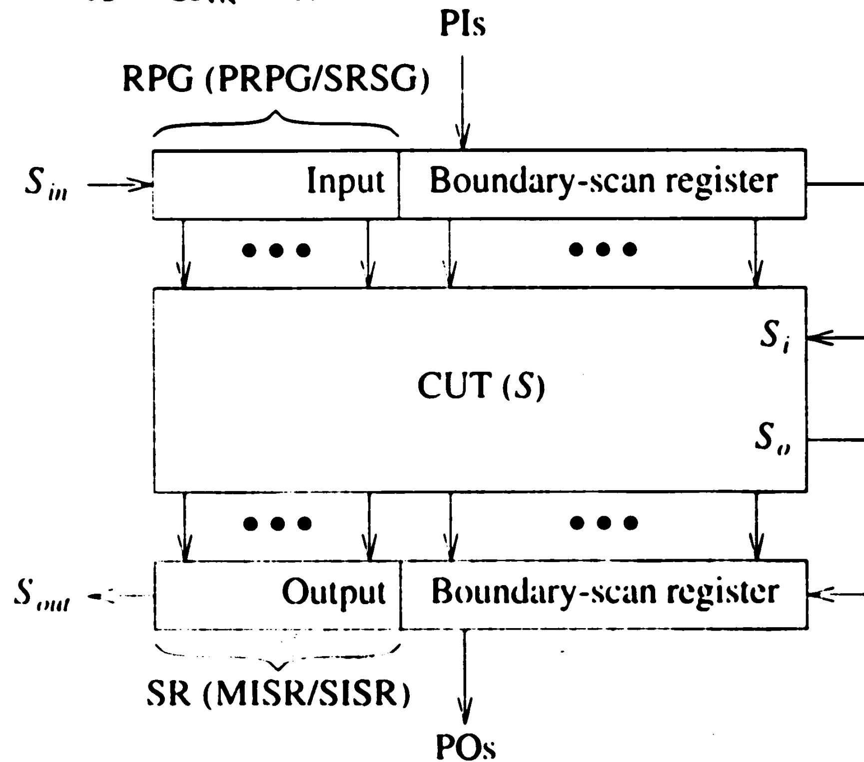
Concurrent BIST (CBIST)

- CUT must be combinational logic
- Supports both off-line & on-line BIST



Centralized & Embedded Architecture with Boundary Scan (CEBS)

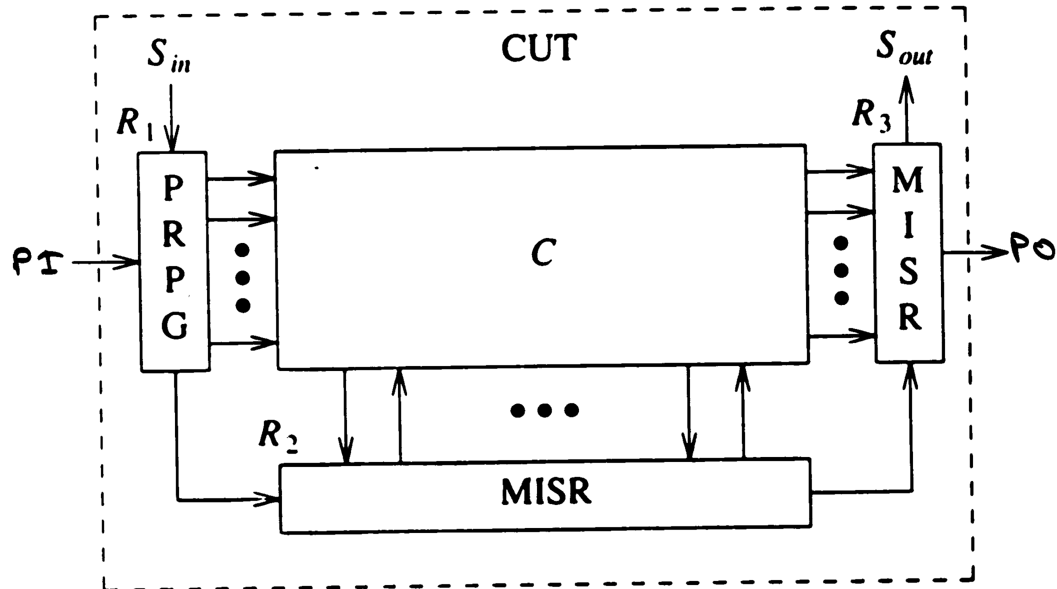
- First r bits of boundary scan register act as a PRPG and a SRSG
- Last s bits of boundary scan register act as both MISR and SISR.



- Testing process:
  1. Scan registers are seeded
  2. RPG loads scan path with pseudo random test data
  3. Scan path registers loaded with system data except SR
  4. Scan path is again loaded with pseudorandom test data while SR operates in SISR mode compressing data from scan path

Random Test Data (RTD) BIST Architecture

- Distributed and embedded BIST
- Boundary scan
- Test per clock

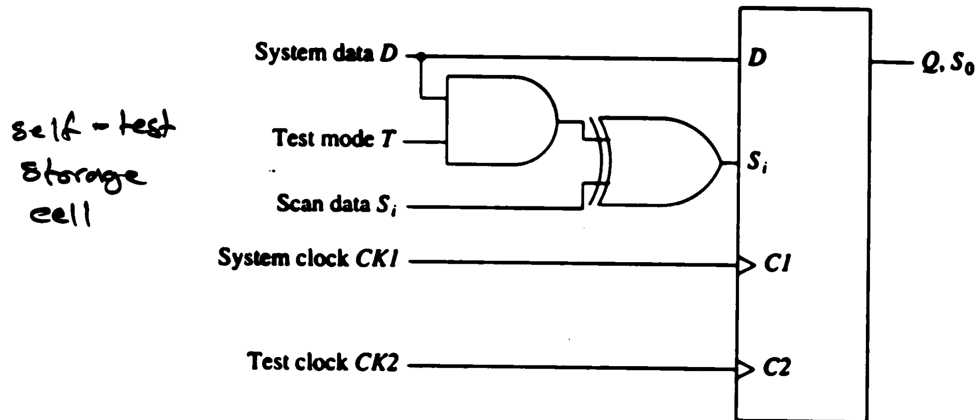


1. Load R1, R2, and R3 by scan in
2. Test the circuit: For each clock
    - R1 & R2 generate new test patterns
    - R2 & R3 operate as MISR
3. Scan out content of R3 & R2

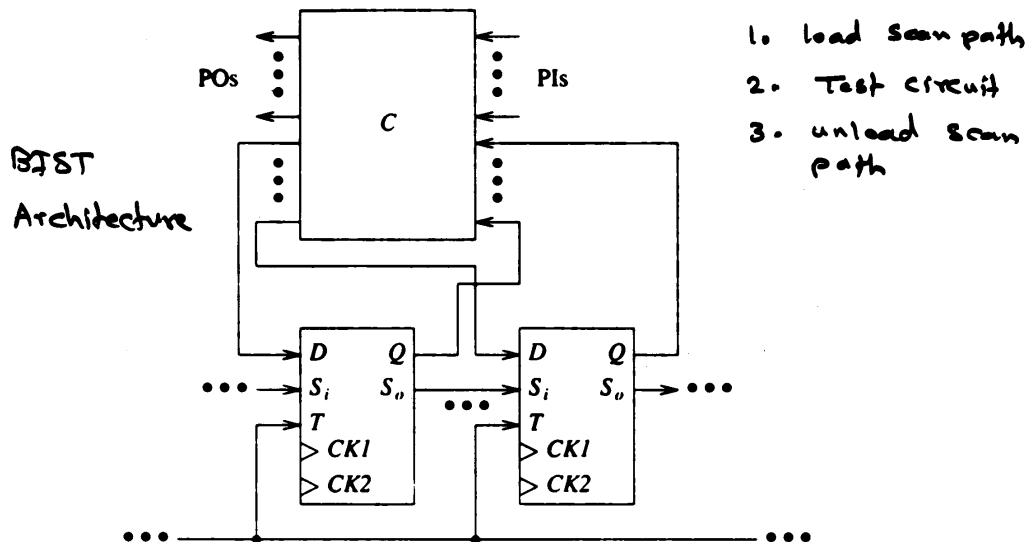
Simultaneous Self-Test (SST)

- Each storage cell is converted to a self-test storage cell
- Features a test per clock

self-test storage cell



BIST Architecture



1. load scan path
2. Test circuit
3. unload scan path