Authors List:

- Camelia Hora @ Eindhoven Univ. of Technology
- Rene Segers @ Philips Semiconductors
- Stefan Eichenberger @ Philips Semiconductors
- Maurice Lousberg @ Philips Research Labs

Paper Title:

# “An Effective Diagnosis Method to Support Yield Improvement”

Presented By: Ihab Hawari

# Abstract


- The ability to achieve and maintain high yield levels depends on the capability of detecting, analyzing and correcting repetitive failure mechanisms.
- In this paper, a statistical fault diagnosis method based on using only the first or the first few failing test vectors is presented.
- The new approach is analyzing the failing vectors from an entire lot and produces a finite list of suspect locations, which are then subjected to further statistical and physical analysis.

# Introduction

- Manufacturing yield in the semiconductor industry is an economic parameter of paramount importance.
- Indeed, the ability to rapidly achieve high yields has become a crucial deciding factor on the economical viability of the business.
- Normally, whenever a new manufacturing process is introduced, the yield is low to start with.
- A rapid yield ramp-up phase then follows which finally stabilizes at a high level in volume production.

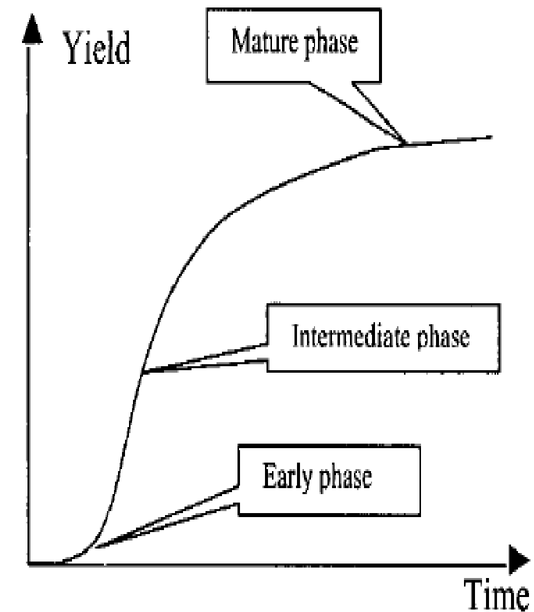

Fig.1. Yield learning phases

- Three distinctive sets of activities are involved in the process of improving the yield:
  - the detection of yield loss.
  - the identification of the failure source (defect diagnosis) and
  - the corrective actions.
- Causes that lead to a loss in yield:
  - Human errors,
  - equipment failure,
  - instability of process parameters and
  - material inhomogenities
- Obviously, all causes must be
  - identified, characterized and appropriate corrective actions taken.

- In-line inspection, parameter evaluation using special tests structures [I] and memories [2,3] are mainly used in the first two phases of the yield learning process as means for detecting and identifying yield loss.
- The special test structures are designed taking into consideration known failure mechanisms (derived from process development and from previous products), as well as special characteristics of a product.
- Global defects, such as for example a smaller thickness of the oxide layer, can he detected and quickly diagnosed using such test structures.

- It is based on the development of statistical diagnosis approach to support fast yield improvement activities.
- The method identifies repetitive failure mechanisms that appear in the logic part of the design.
- It uses the final wafer test results as input data.
- By combining the input data with the layout information, it then highlights the “hot spots” of the device.

# Diagnosis Algorithm Description

- A dictionary based approach has been chosen which can be created off-line using fault-simulation
- The fault model used to create the fault dictionary is stuck-at-fault model
- Only the first few failing test vectors are applied.
- The max: size of fault dictionary signature is set at 100 test vectors

# Diagnosis Algorithm Description

- Input data to statistical diagnosis algorithm are the few failing test vectors from the tester and the fault dictionary
- The algorithm searches in the fault dictionary for the s-a faults detected by the test vector that failed on the tester.
- For each failing die, an output list of suspected failing nets is produced.
- Diagnosis algorithm is the same as in [10]

# Experimental Setup

- The device chosen is 75K gates IC manufactured at Philips with 0.25 um technology
- Two parameters were computed
  - Hit Rate: (the no. of dies which have found correct failing net) / (no. of dies analyzed)
  - Signal/Noise Ratio: (the no. of correctly reported failing nets) / (no. of incorrectly reported nets)
- Performance = HR * SNR

# Performance Results

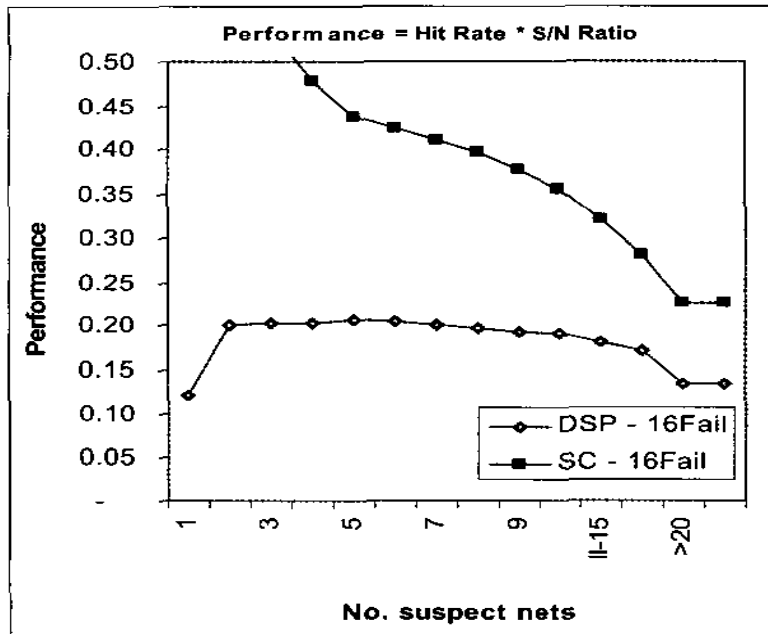


Fig. 5. Performance analysis results

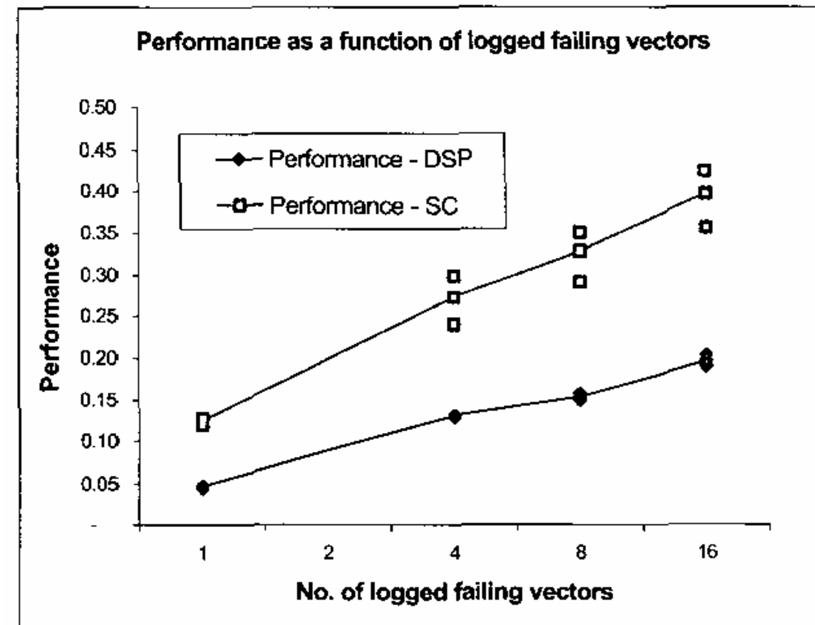


Fig 6. Performance analysis results

Increasing S/N Ratio by discarding the devices for which output list has a number of suspect nets above certain limit ***n***.

# Conclusions

- Develop a statistical diagnosis method supporting (low) yield analysis improvement.
- The method brings statistical analysis capabilities for the domain of random logic rather than regular structure like memories.
- The method is a powerful because it is quickly detect repetitive failure.
- Correlation between in-line inspection and electrical failure analysis can now be performed in a production environment without being penalized by a long test time due to extensive data logging.

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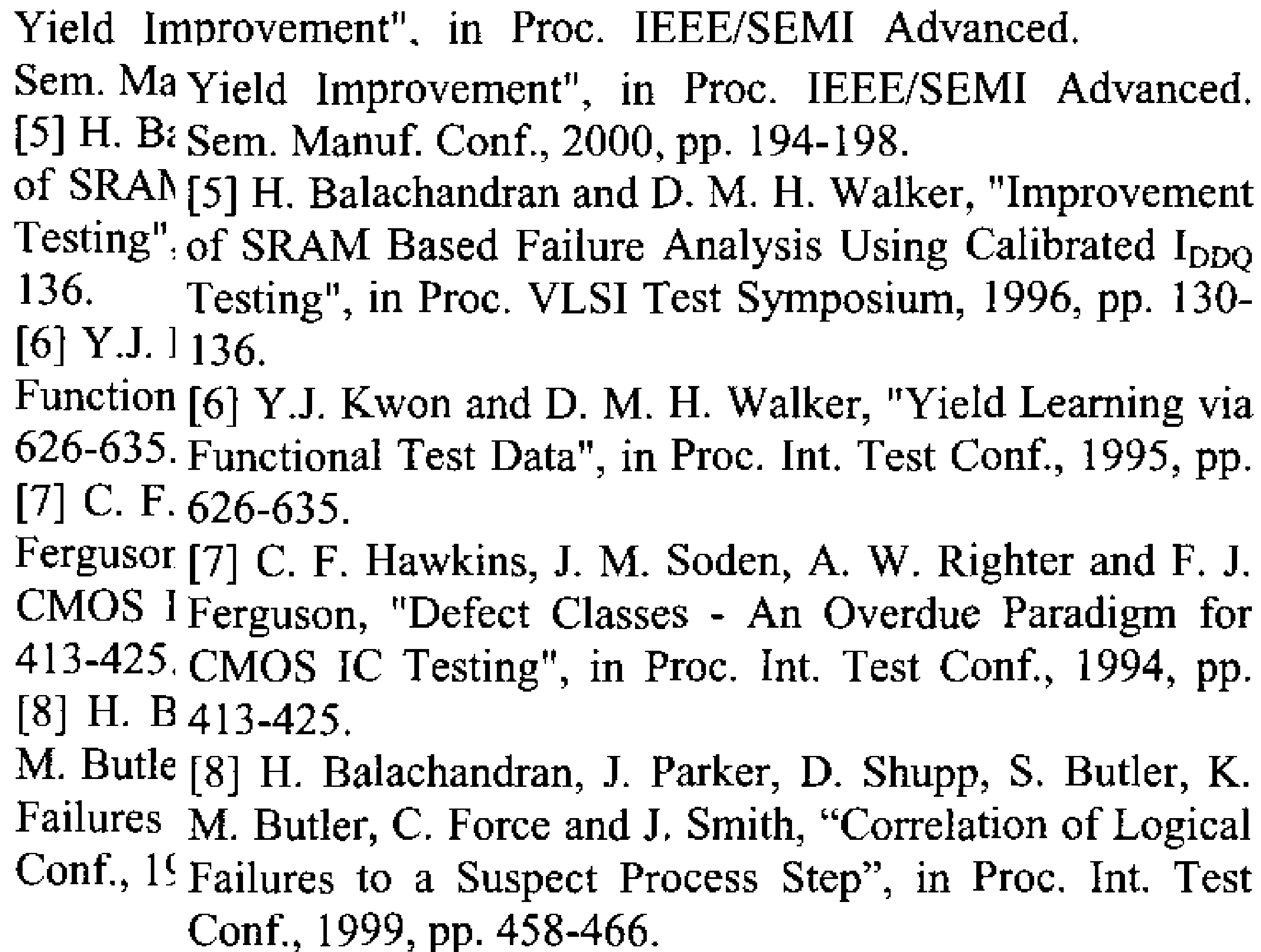

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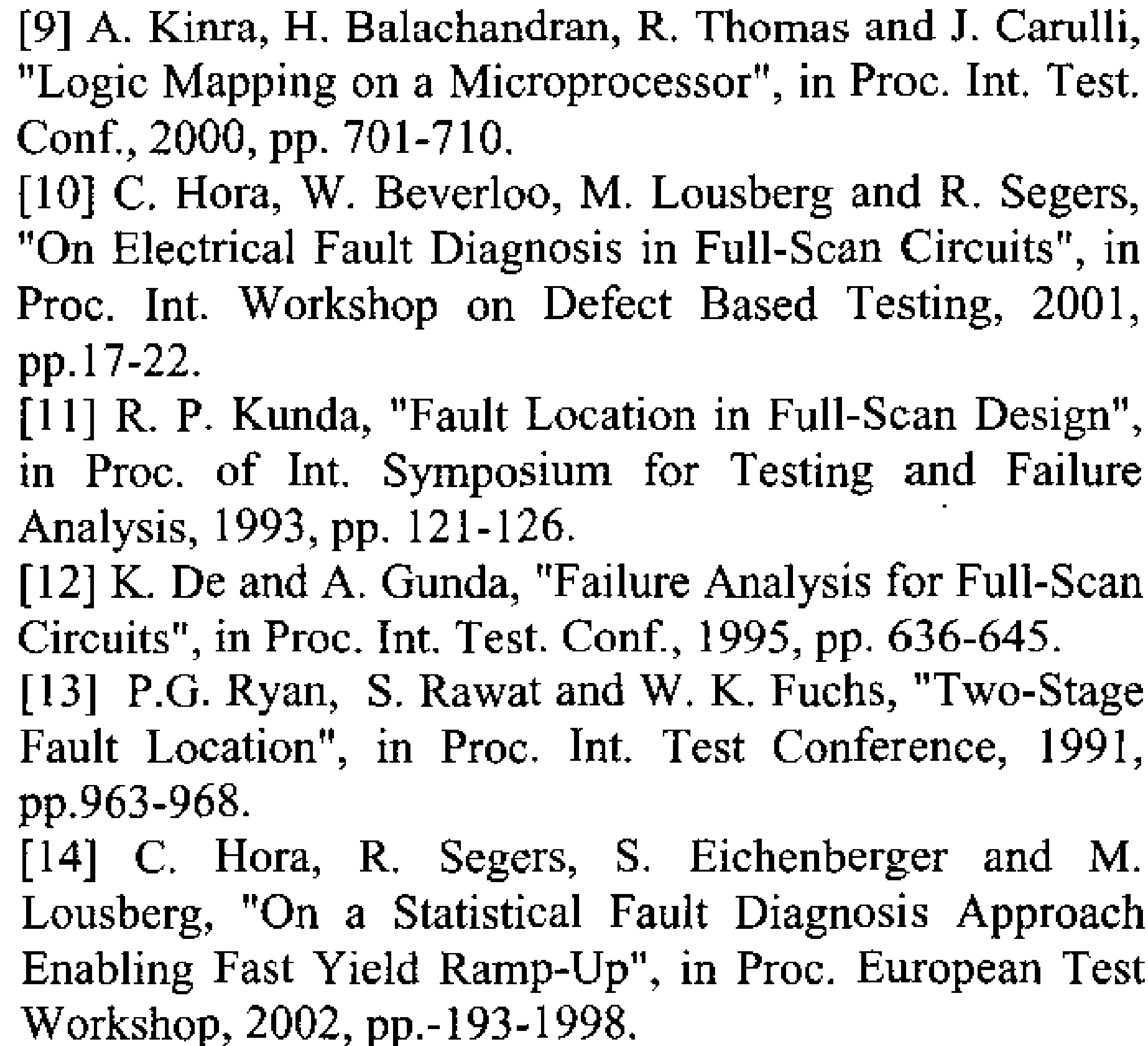

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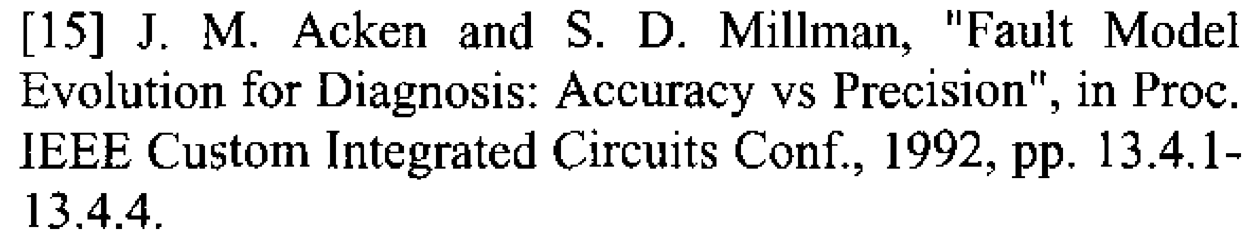
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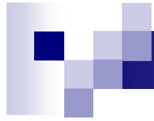

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