COE 561, Term 061

Digital System Design and Synthesis

Course Project

The list of course projects proposed for this term are as shown below. In each project, the main objective of the project and the expected team members are specified. Each student must select a project according to the deadlines specified below.

1. Efficient Power Cost Measure for State Assignment [2 students]

Recently, a new power cost measure for state assignment has been proposed. State assignment for low power utilizing this measure has resulted in better results than previously proposed measures. However, there is still room for improvement. In this project, the students will explore ideas for improving this measure. Then, this measure will be implemented and utilized for state assignment for low power based on existing state assignment algorithms. Working on this project requires knowledge of C language. Results of this work could result in paper publication.

2. Efficient Testability Cost Measure for State Assignment [2 students]

Recently, a new testability cost measure for state assignment has been proposed based on checking circuit initializability and loop count. While this measure has provided excellent results in most cases, for some circuits the generated solutions were uninitializable. In this project, the students will analyze these cases thoroughly to find out the main reason for this. Based on the identified reasons, the cost measure will be modified and then tested and compared with the previous solution. Working on this project requires knowledge of C language. Results of this work could result in paper publication.

3. Design of Reliable Digital Systems based on Triple Modular Redundancy (TMR) and N^2-transistor Structure [2 students]

Nanodevices based circuit design will be based on the acceptance that a certain percentage of devices in the design will be defective. In this project, the students will explore the impact of TMR module size on circuit reliability. Then, the students will explore combining TMR with the recently proposed N^2-transistor Structure and perform experiments to demonstrate the obtained improvements on reliability. In previous work, the fault model used was the transistor stuck-on and stuck-short faults. The students will also explore the use of the bridging fault model and study its impact on reliability. Working on this project requires knowledge of Perl language. Results of this work could result in paper publication.

4. Implementation of ITE DAG [1 student]

This project is of educational nature. The student will implement the ITE procedure and display the obtained ITE DAG in a graphical format. The input to this procedure is the three functions f, g, and h. It can be assumed that these functions will be specified in two-level format for

simplicity. The output will be the reduced ITE DAG. Since this tool is meant for educational purposes, the student is required to have a debugging option where he displays the execution steps of the algorithm in a user friendly format to allow students to follow the algorithm execution.

5. Design of a Digital Circuit from a Behavioral Description [2-3 students]

In this project, the students are required to select a design problem and model the behavior of the circuit to be designed in either Verilog or VHDL. The students are then required to use Synopsys Behavioral Compiler to design two circuits targeting two different optimization measures (i.e. area, delay, power, testability). They should verify that the synthesized solution captures the required behavior of the designed circuits. The students are also required to manually design an architecture for the circuit and then model the design using Verilog or VHDL. Then, the students will use Synopsys Design Compiler to obtain two implementations optimized for two different measures.

Project Deadlines:

Task	Deadline
Project selection	Tuesday, Nov. 14
Project Plan	Sunday, Nov. 19
Progress Report 1	Tuesday, Dec. 5
Progress Report 2	Tuesday, Dec. 19
Final Report & Project Demonstration	Sunday, Jan. 14

Each student group is expected to submit a project plan describing the project tasks, the time planned for each task, and the team members' role in each task. Each group is also required to submit two progress reports describing briefly the progress made so far in the project against planned work, difficulties faces, results obtained so far and the tasks to be performed in the next period. At the end of the project, each group is required to submit a professional report showing the details of all the work performed and demonstrate their project to me.

Project Evaluation Criteria:

Task	Mark
Project Plan	5%
Progress Report 1	5%
Progress Report 2	5%
Project Accomplishments vs. Requirements	60%
Final Report	25%