Term 051

COE 561 Digital System Design and Synthesis

HW# 5

Due date: Sunday, Dec. 18

Q.1. Consider the logic network defined by the following expressions:

$k = (i \cdot j)'$

$j = (d \cdot h)'$

$i = (f \cdot e)'$

$h = (g)'$

$g = (c \cdot f)'$

$f = (a \cdot b)'$

Inputs are *{a, b, c, d, e}* and output is *{k}*. Assume that the delay of inverter gate is 1 and that the delay of the 2-input NAND gate is 2. Also, assume that the input data-ready times are zero except for input *a* which is equal to 2.

(i) Draw the logic network graph and compute the data ready times and slacks for all vertices in the network.

(ii) Determine the topological critical path.

(iii) Suggest an implementation of the function ***k*** to reduce the delay of the circuit and determine the maximum propagation delay in the optimized circuit. Has the area been affected?

Q.2. Determine the number of ROBDDs required to be stored for each of the following library cells for Boolean matching. Justify your answer.

(i) F = a b + b' c.

(ii) F = a b + c d.

(iii) F = a b + c' d'.

Q.3. Consider a library containing the following cells:

Cell	Area Cost
INV	1
NAND2	2
AND2	2.5
NOR2	2
OR2	2.5
AOI21	4
AOI22	4.5

Assume that you have the following network:

i = d'; *j = e';* *k = h';*
l = a b; *m = l + c;* *n = i + j;*
o = f +g; *p = m + n;* *q = o + k;* *r = p q;*

(i) Decompose the given network using the base cells NAND2 and INV.

(ii) Find a minimal cover (in terms of area) based on the given library for each subject graph using dynamic programming approach. Pattern strings for the library cells are given in Fig. 10.8.

(iii) Using the given library, use the sis command ***read_libray*** to read the library. Then, map the network to the library using the sis command ***map –s –m 0***. Compare your solution to the solutions obtained in (iv) & (v). You can save the mapped circuit using the sis command ***write_blif –n***.