**COE 561, Term 091**
**Digital System Design and Synthesis**
**HW# 3**

**Due date: Tuesday, Dec. 29**

**Q.1.** Consider the following function:

$$X = ACE + BCE + AC'D' + BC'D' + DE + F$$

**(i)** Compute all the kernels of *X* using the recursive kernel computation algorithm. Show all the steps.

**(ii)** Compute all the kernels of X based on matrix representation. Compare your answer to the result obtained in (i).

**(iii)** Find a quick factor of *X* by using the first level-0 kernel found. Assume that input variables are sorted in lexicographic order. Determine the number of literals obtained. Compare your solution with the result obtained by running the sis commands ***factor –q x; print_factor; print_stats –f.***

**Q.2.** Consider the following function:

$$X=AC+BC+AD+BD+A'B'C'+A'B'D'+AEF+BEF+AE'F'+BE'F'+A'B'EF'+A'B'E'F$$

**(i)** Compute all double-cube divisors of *X* along with their bases and their weights. Show only double-cube divisors that have non-empty bases.

**(ii)** Apply the fast extraction algorithm based on extracting double-cube divisors along with complements or single-cube divisors with two-literals. Show all steps of the algorithm. Determine the number of literals saved. Compare your solution with the result obtained by running the sis commands ***fx***.

**Q.3.** Consider the logic network defined by the following expressions:

$$X = AB' + A'B;$$
$$Y = XC + A B;$$
$$Z = Y + A';$$

Inputs are {A, B, C} and output is {Z}.

**(i)** Compute the SDC set for node X.

**(ii)** Compute the ODC set for node Y.

**(iii)** Simplify the function of Y using both its ODC and SDC of node X.

**(iv)** Compute the ODC set for node X based on the optimized network on (iii).

**(v)** Simplify the function of X using its ODC.

**(vi)** Apply the sis command ***full_simplify*** and compare the solution obtained with your obtained solution based in (iv).

**Q.4.** Consider the logic network defined by the following expressions:

e=a b d

f =c d

g = e + f

h = a d

i =a' b' d'

j = h + i

k= b d

l =j + k

x =g + l

Inputs are {a, b, c, d} and output is {x}. Assume that the delay of a gate is related to the number of its inputs. Also, assume that the input data-ready times are zero except for input d, which is equal to 2.

**(i)** Draw the logic network graph and compute the data ready times and slacks for all vertices in the network.

**(ii)** Determine the **maximum propagation delay** and the **topological critical path**.

**(iii)** Suggest an implementation of the function ***x*** to reduce the delay of the circuit. What is the **maximum propagation delay** after the modified implementation?