COE 561, Term 091

Digital System Design and Synthesis

First Paper Presentation

Thursday, Dec. 17, 2009

List of Papers:

1. Robert Wille and Rolf Drechsler, "***BDD-based Synthesis of Reversible Logic for Large Functions,***" Proceedings of the 46th Annual Design Automation Conference**,** pp. 270-275, 2009.
2. Nishant Patil, Albert Lin, Jie Zhang, H.–S. Philip Wong and Subhasish Mitra, ***"Digital VLSI Logic Technology using Carbon Nanotube FETs: Frequently Asked Questions,"*** Proceedings of the 46th Annual Design Automation Conference**,** pp. 304-309, 2009.
3. Hsuan-Po Lin, Jie-Hong R. Jiang and Ruei-Rung Lee, ***"To SAT or Not to SAT: Ashenhurst Decomposition in a Large Scale,"*** IEEE/ACM International Conference Computer-Aided Design, pp. 32-37, 2008.
4. Alan Mishchenko, Robert Brayton and Satrajit Chatterjee, ***"Boolean Factoring and Decomposition of Logic Networks,"*** IEEE/ACM International Conference Computer-Aided Design, pp. 38-44, 2008.
5. Tsutomu Sasao, ***"On the Numbers of Variables to Represent Sparse Logic Functions,"*** IEEE/ACM International Conference Computer-Aided Design, pp. 45-51, 2008.
6. John Backes, Brian Fett and Marc D. Riedel, ***"The Analysis of Cyclic Circuits with Boolean Satisfiability,"*** IEEE/ACM International Conference Computer-Aided Design, pp. 143-148, 2008.
7. I. Brzozowski and A. Kos, ***"Two-Level Logic Synthesis for Low Power Based on New Model of Power Dissipation,"*** IEEE Design and Diagnostics of Electronic Circuits and Systems, pp. 1-6, 2007.
8. Joao Marques-Silva, ***"Practical Applications of Boolean Satisfiability,"*** Proceedings of the 9th International Workshop on Discrete Event Systems, pp. 74-80, 2008.

No.	Paper Title	Presenters
1	***Digital VLSI Logic Technology using Carbon Nanotube FETs: Frequently Asked Questions***	Suli ADENIYE Mohammed YAHAYA
2	***Practical Applications of Boolean Satisfiability***	Ahmed B. ALI Mohammed Salout
3	***BDD-based Synthesis of Reversible Logic for Large Functions***	Ismail Kishta Saad Khan
4	***On the Numbers of Variables to Represent Sparse Logic Functions***	AHAMED ABDELSATIR
5	***The Analysis of Cyclic Circuits with Boolean Satisfiability***	ABDULRAHMAN IDLBI
6	***Boolean Factoring and Decomposition of Logic Networks***	GHALIB ALHASHIM