*KING FAHD UNIVERSITY OF PETROLEUM & MINERALS*
*COLLEGE OF COMPUTER SCIENCES & ENGINEERING*

## *COMPUTER ENGINEERING DEPARTMENT*

### COE 561: Digital System Design and Synthesis
### Syllabus - Term 041

## Catalog Description :

Design representations, levels of abstraction & domains, Digital system design methodologies, Hardware Description Languages (HDLs), Modeling of Digital Systems using HDLs, High Level synthesis – Internal representation (CDFG), Scheduling, Allocation & binding, Controller and Data Path synthesis, Logic Synthesis – Two-level & Multi-level logic synthesis, Sequential logic synthesis (FSM synthesis), Technology Mapping- Library binding approaches, some case studies. The course emphasizes hands on experience through the use of available synthesis tools.

***Pre-requisite :*** COE 308 or Equivalent

**Instructor** Dr. Aiman H. El-Maleh Room: 22/318 Phone: 2811
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## Text Book :

- Synthesis and Optimization of Digital Circuits – Giovanni De Micheli, McGraw Hill International edition, ISBN –0-07-113271-6, 1994.

## References:

**Books:**

- Logic synthesis & verification algorithms – Gary D. Hachtel, Fabio Somenzi, Kluwer Academic Publishers; ISBN: 0792397460, 1996.
- Logic synthesis and verification, S. Hassoun and T. Sasao, Kluwer Academic Publishers, 2002.
- Logic Synthesis Using Synopsys – Pran Kurup, Taher Abbasi, Second Edition, Kluwer Academic Publishers, 1996.
- VHDL: Analysis and Modeling of Digital Systems, Navabi, McGraw-Hill, Inc., 2nd edition, 1998.

**Journals:**

IEEE Transactions on CAD
IEEE Transactions on VLSI Design
IEEE Transactions on Computers

**Conference Proceedings:**

Design Automation Conference (DAC)
International Conference on Computer Aided Design (ICCAD)
Design Automation and Test in Europe (DATE)
International Conference on Computer Design (ICCD)

## Tools:

We will be using the following tools in this course: SIS package, Modelsim, Synposys synthesis tools, and Xilinx tools.

## Detailed Syllabus:

- **INTRODUCTION**

  - Microelectronics, semiconductor technologies, microelectronic design styles, design representations, levels of abstraction & domains, Y-chart, system synthesis and optimization, issues in system synthesis. **0.5 week**

- **MODELING OF DIGITAL SYSTEMS**

  - Introduction to Hardware description languages(HDLs). Hardware Description and design using VHDL. Basic modeling concepts, Language elements, Behavioral modeling, Dataflow modeling, Structural modeling, some hardware modeling examples. **1.5 week**

- **LOGIC SYNTHESIS** **6.5 weeks**

  - Introduction to logic synthesis
    - Boolean functions representation, Binary Decision Diagrams, Satisfiability and Cover problems **0.5 week**
  - Two-level logic synthesis and optimization
    - Logic minimization principles, Exact logic minimization, Heuristic logic minimization, The Espresso minimizer, Testability properties of two-level circuits. **1 week**
  - Multi-level logic synthesis and optimization
    - Models and transformations of combinational networks: elimination, decomposition, extraction. The algebraic model: algebraic divisors, kernel set computation, algebraic extraction and decomposition. The Boolean model: Don't care conditions and their computations, input controllability and output observability don't care sets, Boolean simplification and substitution. Optimization based on redundancy addition and removal. Transduction, Global flow. Testability properties of

multilevel circuits. Synthesis of minimal delay circuits. Rule-based systems for logic optimization. **2 weeks**

- Sequential Logic Synthesis
    - Introduction to FSM Networks, Finite state minimization, state encoding: state encoding for two-level circuits, state encoding for multilevel circuits, Finite state machine decomposition, Retiming, Implicit finite state machine traversal methods, and Testability consideration for synchronous sequential circuits. **2 weeks**
- Technology Mapping
    - Problem formulation and analysis, Library binding approaches – Structural matching, Boolean matching, Covering & Rule based approach, Case studies – Mapping the design onto FPGAs. **1 week**

- **HIGH LEVEL SYNTHESIS** **6.5 weeks**

    - Introduction to High level synthesis
    - Design representation and transformations
        - Design flow in high level synthesis, HDL compilation, internal representation (CDFG), data flow and control sequencing graphs, data-flow based transformations. **0.5 week**
    - Architectural Synthesis
        - Circuit specifications: resources and constraints, scheduling, binding, area and performance optimization, datapath synthesis, control unit synthesis, synthesis of pipelined circuits. **2 weeks**
    - Scheduling
        - Unconstrained scheduling: ASAP scheduling, Latency-constrained scheduling: ALAP scheduling, time-constrained scheduling, resource constrained scheduling, Heuristic scheduling algorithms: List scheduling, force-directed scheduling. **2 weeks**
        - Allocation and Binding: resource sharing, register sharing, multi-port memory binding, bus sharing and binding, unconstrained minimum-performance-constrained binding, concurrent binding and scheduling. **2 weeks**

## Grading Policy

- Assignments 15%
- Midterm 25%
- Implementation Project 20%
- Survey Project 15%
- Final 25%

## Survey Project Guidelines

- The survey project involves the following main tasks :

  - Literature survey of 5 papers on a selected recent topic.
  - At least **two** of the covered papers should be journal papers
  - At least **one** of the covered papers should be published within the last two years.
  - Preparation of a report describing the surveyed papers.
  - Presentation of the report.
  - Evaluation of the survey project will strongly depend on the understanding of the covered papers and the clarity of the prepared report.

- Suggested topics for the term paper are given below:

  - Recent advances in SAT solvers
  - Recent advances in technology mapping
  - Synthesis of cyclic combinational logic circuits
  - Quantum logic synthesis
  - Domino logic synthesis
  - On-Chip logic minimization
  - Networks on chip design methodology
  - State assignment for testability
  - State assignment for low power
  - Low-power embedded system design
  - Synthesis of asynchronous logic
  - High-level synthesis of asynchronous systems
  - Design paradigm for nanotechnologies
  - Architecture synthesis for deep submicron systems on Chip
  - Synthesis for noise and manufacturability
  - Timing-driven system synthesis
  - Synthesis of pipelined circuits
  - Hardware/Software Co-design
  - SOC Design Methodologies / Design Challenges / Design Languages
  - Power Co-estimation techniques for SOC
  - Co-synthesis of Hardware & Software for Digital Embedded Systems
  - Hardware-Software Partitioning and Scheduling algorithms for Dynamically Reconfigurable Embedded Systems
  - ASIP (Application Specific Integrated Processors) Design Methodologies

- Each student is required to select a separate topic from the above list by **Sunday, 10th October 2004.**
- Last date for Submission of the survey project: **Sunday, 28th December 2004**
- Maximum duration of the presentation will be 30 minutes for each student. The student will be asked to present two of the covered papers only. The papers to be presented will be selected by the instructor.

## Implementation Project Guidelines

The student can choose one of the following options:

**a. Modeling and Synthesis**

- Mini-project involves synthesis of a digital system (fairly good complexity) for a particular application using Synopsys and Xilinx FPGA tools.
- Each student is required to select a separate design problem and carry-out the work independently.
- Modeling and synthesis project involves the following main-tasks :

    - Modeling of the digital system using VHDL

    - Simulation using ModelSim to verify functionality

    - Synthesis using Synopsys/XST tools and estimating area, delay and power

    - Mapping the design onto FPGAs using Xilinx tools

- Deliverables :

    - A Project Report with complete design description, VHDL code, simulation & synthesis results, FPGA placement & routing statistics in terms of number of LUTs and IOBs used and the delay along the critical path(s).
    - Demonstrate the working of your design on a FPGA prototype board.

**b. Algorithm Implementation**

    - The student selects a particular synthesis algorithm and implements it.

- Submit a proposal on the implementation project selected by **Sunday, 17$^{h}$ October 2004.**

- Last date for submission of implementation will be **Sunday**, **2$^{nd}$ January 2005**.