# KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
## *COMPUTER ENGINEERING DEPARTMENT*
### COE 561: Digital System Design and Synthesis
### Term 081 Lecture Breakdown

| | Date | Topics | Ref. |
|---|---|---|---|
| 1 | U 12/10 | Syllabus, **Introduction**: Microelectronics Design Problems, Microelectronics Design Styles. | Chapter 1 |
| 2 | T 14/10 | Dealing with design complexity, Design domains and levels of abstractions, Digital system design, Design vs. synthesis, Digital system design cycle, Synthesis process. High-level synthesis, Design and evaluation space, Combinational design space example, Architecture design space example, Pareto Optimality. | Chapter 1 |
| 3 | U 19/10 | **Logic Synthesis Background**: Boolean Algebra, Boolean Functions, Shannon's Theorem. Unate functions. | 2.5 |
| 4 | T 21/10 | Boolean difference, Consensus, Smoothing, Orthonormal Basis Expansion. Representation of Boolean functions, **Binary Decision Diagrams.** | 2.5 |
| 5 | U 26/10 | Reduced Binary Decision Diagrams, **ITE DAGs**. | 2.5 |
| 6 | T 28/10 | Applications of ITE DAGs. **Satisfiability**, Satisfiability Formulation as Zero-One Linear Programming (ZOLP) Problem, Minimum Covering Problem, Minimum-Vertex Cover Example, Minimum-Edge Cover Example, Covering Problem Formulated as Satisfiability Problem, **Branch & Bound Algorithm**. Covering reduction strategies. | 2.5 |
| 7 | U 2/11 | Branch and Bound Exact Covering Algorithm, Bounding function. **Two-level minimization**: Programmable Logic Arrays, Minimal or irredundant cover, Minimal cover w.r.t. 1-implicant containment. | 2.5 & Chapter 7 |
| 8 | T 4/11 | No class. | |
| | S 8/11 Makeup | Prime implicant, Prime cover, Essential prime implicant. **Positional cube notation**, Operations on logic covers: intersection, supercube, distance, cofactor, Sharp. | Chapter 7 |
| 9 | U 9/11 | Disjoint Sharp, Consensus, Computation of all prime implicants, Tautology, Containment. | Chapter 7 |
| 10 | T 11/11 | Containment, Complementation. **Exact two-level minimization**, ESPRSSSO-EXACT. **Heuristic minimization**, Heuristic minimization operators: Expand. | Chapter 7 |

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| | Th. 13/11 | **Major Exam I** | |
| 11 | U 16/11 | Heuristic minimization operators: Reduce, Irredundant, Reshape. Expand heuristics. | Chapter 7 |
| 12 | T 18/11 | Expand heuristics. | Chapter 7 |
| | T 18/11 | **Last day dropping with W** | |
| 13 | U 23/11 | Expand heuristics, Reduce, Irredundant. | Chapter 7 |
| 14 | T 25/11 | Irredundant, Essentials. Espresso Algorithm. Testability of Two Level circuits. | Chapter 7 |
| 15 | U 30/11 | Logic Network, Network optimization, Area Estimation. **Mutlilevel transformations**: Elimination, Decomposition, Factoring, Extraction, Simplification, Substitution. Elimination algorithm. **Algebraic model**. | Chapter 8 |
| 16 | T 2/12 | **Algebraic model**, Algebraic division algorithm, Substitution algorithm, Extraction, Kernels. | Chapter 8 |
| | | **E i d A d h a H o l i d ay** | |
| 17 | U 14/12 | Extraction, Kernels, Kernels computation. **Kernel Set Computation**, Recursive Kernel Computation, Matrix Representation of Kernels. | Chapter 8 |
| 18 | T 16/12 | Single-Cube Extraction, Multiple-cube extraction, **Decomposition**. **Factorization** Algorithm: quick & Good Factoring. **Fast Extraction** Algorithm: Double-cube divisors and single-cube divisors | Chapter 8 |
| 19 | U 21/12 | **Fast Extraction** Algorithm: Double-cube divisors and single-cube divisors, Boolean Methods, Controllability & Observability don't care conditions. **Satisfiability don't care** conditions, Controllability don't care computation. | Chapter 8 |
| | M 22/12 | **1st Paper Presentation** | |
| 20 | T 23/12 | Controllability don't care computation, Observability don't care conditions computation. | Chapter 8 |
| 21 | U 28/12 | Transformations with don't cares. Optimization and perturbations, synthesis and testability, **Synthesis for testability**. | Chapter 8 |
| 22 | T 30/12 | timing issues in multilevel logic optimization, **delay modeling**, topological critical path. False path problem, Algorithms for delay minimization, Transformations for delay reduction | Chapter 8 |
| | | **Last day dropping all courses with W** | |
| 23 | U 4/1 | More refined delay models, Speedup algorithm. **Library Binding**: Library Models, Major Approaches. | Chapter 8 & 10 |
| 24 | T 6/1 | **Library Binding**: Rule-based library binding, Algorithms for library binding, Partitioning, Decomposition, Matching, Covering. | Chapter 10 |
| 25 | U 11/1 | Tree-based matching. **Tree-based covering,** | Chapter 10 |

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| | | **Minimum Delay Cover**: constant and load-dependent delays, **Boolean matching**. | |
| 26 | T 13/1 | **Boolean matching**: Signatures and Filters. **Sequential Logic Synthesis**: Modeling Synchronous circuits, **State minimization** for completely and incompletely-specified FSMs. | Chapter 9 & 10 |
| | Th. 15/1 | **Major Exam II** | |
| 27 | U 18/1 | **State Assignment**. State encoding for two-level models. Symbolic minimization, **Input encoding problem.** | Chapter 7 & 9 |
| 28 | T 20/1 | **Input encoding problem.** Dichotomy theory, Exact & Heuristic input encoding. **Output and mixed encoding**, Covering and Disjunctive relation. | Chapter 7 & 9 |
| | | **Dropping all courses with WP/WF** | |
| 29 | U 25/1 | State encoding for two-level implementation, Synchronous logic network, **Retiming**. **Architectural-level synthesis**, Data-flow graphs, **Sequencing graphs**, Behavioral optimization of sequencing graphs. Synthesis in the temporal domain: **Scheduling**, Synthesis in the Spatial domain: **Binding.** | Chapter 7 & 9 & 3 & 4 |
| 30 | T 27/1 | Scheduling Models, Minimum latency unconstrained scheduling, ASAP & ALAP scheduling, Latency Constrained Scheduling, Scheduling under Resource Constraints, List Scheduling Algorithm for Minimum Latency, List Scheduling Algorithm for Minimum Resource Usage, Algorithmic Solution to the Optimum Binding Problem, Register Binding Problem. | Chapter 5 & 6 |
| | Th. 29/1 | **2nd Paper Presentation** | |