Name: **Id#**

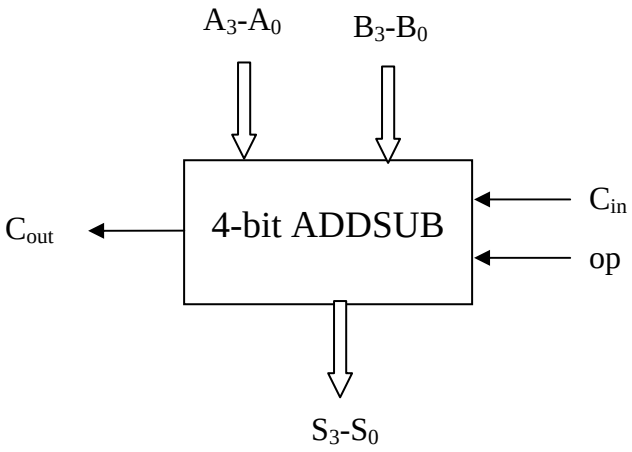
COE 405, Term 021

Design & Modeling of Digital Systems

Quiz# 1

Date: Monday, October 7, 2002

Q.1. It is required to model a 4-bit adder/subtractor. The interface description of the 4-bit adder/substractor is shown below, where **op** determines the operation. When op=0, the operation A+B is performed, otherwise A-B is performed.



(i) Describe an Entity **FAS** for a 1-bit full adder/subtractor.

(ii) Model an Architecture **Conc** for this 1-bit FAS using concurrent statements.

(iii) Describe an Entity **AS4** for a 4-bit adder/subtractor using the interface names given above.

(iv) Model Architecture **Struct** for the 4-bit adder/subtractor (**AS4**) using instantiations of the Entity **FAS**.