

## COE 405, Term 031

### Design & Modeling of Digital Systems

#### HW# 5

Due date: Tuesday, Dec. 16, 2003

- Q.1.** It is required to model in VHDL arithmetic and logic unit (ALU) with inputs A and B and output C, that can perform any of the following functions shown below based on the three selection lines AS2, AS1, and AS0:

AS2	AS1	AS0	Operation
0	0	0	$C=A+B$
0	0	1	$C=A-B$
0	1	0	$C=A+1$
0	1	1	$C=A-1$
1	0	0	$C=B$
1	0	1	$C=\text{NOT } A$
1	1	0	$C= A \text{ AND } B$
1	1	1	$C= A \text{ OR } B$

Assume that all the inputs and outputs are of type `std_logic`. Model the ALU to be of generic size such that the size of the ALU is specified by a generic map.

- (i) Simulate a 4-bit ALU to verify the correctness of your model and include simulation results.
  - (ii) Synthesize a 2-bit ALU using Xilinx FPGA tools and demonstrate the functionality of your design.
- Q.2.** Write a VHDL description for a CMOS memory element with read/write control, enable, and a shared input-output line. When enabled and  $rw = 1$ , the output is driven by the memory. When enabled and  $rw = 0$ , the input will be written into the memory. Use `qit` type.
- (i) Using this memory element, write a structural VHDL description for modeling a  $2^n \times m$  bit memory array ( $2^n$  rows and  $m$  columns) that has  $n$  bit address size and  $m$  bit data size. All input-output lines in a column are wired. The address and data sizes should be generic. Use an  $n \times 2^n$  row decoder for decoding the address.
  - (ii) Simulate a  $2^3 \times 4$  (i.e. 8 x 4 with 3-bit address) memory and verify its correct functionality by writing and reading from all addresses.
  - (iii) Synthesize a  $2^3 \times 4$  (i.e. 8 x 4 with 3-bit address) memory and verify its correct functionality using Xilinx FPGA tools.