COE 405, Term 021

Design & Modeling of Digital Systems

HW# 5

Due date: Monday, Dec. 16, 2002

Q.1.

(i) Write a function for the carry output of a full-adder.

(ii) Write a function for the sum output of a full adder.

(iii) Using the carry and sum functions, write a functional description of a full-adder. Use an entity declaration with *a*, *b*, and *ci* inputs and *s* and *co* outputs. In the functional architecture of this entity, include the necessary functions. Use 21- and 18-ns delays for the sum and carry outputs, respectively.

Q.2. 6.5

Q.3. Using *bin2int* and *int2bin* in the *basic_utilities* package write a function, *inc_bin,* that uses a binary input parameter and returns a binary value. The return value is the increment of the input parameter. Define the *basic_utitlities* package to include *bin2int* and *int2bin* and use it.

Q.4.

(i) Write an entity declaration and an *average_delay* architecture for an exclusive-OR gate with a *tplh* of 9 ns and a *tphl* of 7 ns. The entity declaration should contain generics for the timing parameters with the specified default values.

(ii) Using an XOR gate and 2-input NAND gate, write a gate-level description for a full-adder. Use a configuration specification to use the XOR and 2-input gate with *average_delay* architecture with generic map aspects to override the default values of the timing parameters of all gates with 11 ns.

(iii) Using an XOR gate and 2-input NAND gate, write a gate-level description for a full-adder. Write a configuration declaration on top of the full-adder to use the XOR and 2-input gate with *average_delay* architecture with generic map aspects to override the default values of the timing parameters of all gates with 11 ns.

(iv) Use generate statements to describe an 8-bit adder using the full-adder described in (iii). Write a configuration declaration on top of this adder to use the XOR and 2-input NAND gate with *average_delay* architecture. Using this configuration declaration, specify *tplh* and *tphl* of 10 ns and 11 ns for NAND2 and 11 ns and 13 ns for XOR.