

March 29, 2007

COMPUTER ENGINEERING DEPARTMENT

COE 405

DESIGN & MODELING OF DIGITAL SYSTEMS

Major Exam I

Second Semester (062)

Time: 1:00-3:00 PM

OPEN BOOK EXAM

Student Name : _____

Student ID. : _____

Question	Max Points	Score
Q1	25	
Q2	25	
Q3	50	
Total	100	

Dr. Aiman El-Maleh

[25 Points]

(Q1) Given the following signal assignments, show all transactions placed on each signal. At each event, show transactions that are appended, overwritten, and are expired. Show the resulting waveforms on the signals.

Architecture Concurrent of Q1 IS

Signal X, X1, X2, X3, X4: BIT;

Begin

X <= '1', '0' **AFTER** 5 ns, '1' **AFTER** 9 ns, '0' **AFTER** 20 ns;

X1 <= X **AFTER** 5 ns;

X2 <= **Transport** X **AFTER** 5 ns;

X3 <= X **AFTER** 6 ns;

X4 <= **Reject** 3 ns **Inertial** X **AFTER** 6 ns;

End Concurrent;

	Time						
X	Current Value						
	Projected Waveform						
X1	Current Value						
	Projected Waveform						
X2	Current Value						
	Projected Waveform						
X3	Current Value						
	Projected Waveform						
X4	Current Value						
	Projected Waveform						

	Time						
X	Current Value						
	Projected Waveform						
X 1	Current Value						
	Projected Waveform						
X 2	Current Value						
	Projected Waveform						
X 3	Current Value						
	Projected Waveform						
X 4	Current Value						
	Projected Waveform						

[25 Points]

(Q2) It is required to write a structural VHDL model to implement the following equation:

$$X = A B + A C + \overline{A} \overline{B}, \text{ where } A, B, \text{ and } C \text{ are primary inputs and } X \text{ is a primary output.}$$

Assume that the work library has the following entities:

```
Entity inv is
  port (i1: IN bit; o1: OUT bit);
End inv;
Entity nand2
  port (i1, i2: IN bit; o1: OUT bit);
End nand2;
Entity nand3
  port (i1, i2, i3: IN bit; o1: OUT bit);
End nand3;
```

- i) Describe an Entity **Q2** showing the interface signals.
- ii) Describe an architecture **Sol1** for the Entity using the components **n1**, **n2**, and **n3** corresponding to an inverter, 2-input nand gate and 3-input nand gate respectively. Configure your design to use Entity **inv** with Architecture **single_delay** for **n1**, Entity **nand2** with Architecture **single_delay** for **n2**, and Entity **nand3** with Architecture **single_delay** for **n3**.
- iii) Change the configuration statement in (ii) to configure your design to use Entity **nand3** with Architecture **single_delay** for all components **n1**, **n2**, and **n3**.

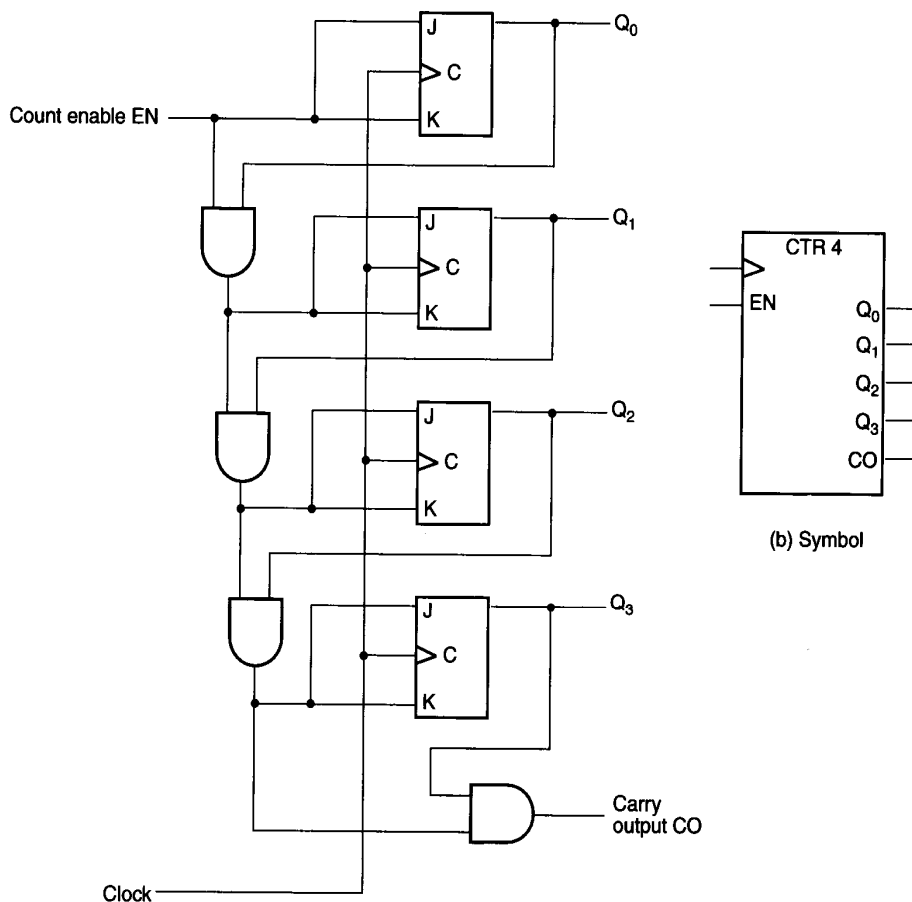
(Q3) A JK flip-flop with the following interface declaration is given:

ENTITY JKFF IS

PORT (J, K, RESET, CLK : IN BIT; Q : OUT BIT);

END JKFF;

- i) Write a behavioral model for the JK flip-flop assuming that it is rising-edge triggered and that the reset is asynchronous.
- ii) An up-counter can be designed using JK flip flops in a modular way as shown below (one JK-FF and one AND gate). Using the JK flip-flop modeled in (i), model a 1-bit modular binary counter.
- iii) Based on the 1-bit modular binary counter modeled in (ii), model a generic N-bit binary ripple up counter as shown below using Generate statement. Show the Entity description and Architecture of this counter using a Generic statement for the counter size. The counter does not count when the count enable is 0. Otherwise, it counts up on the rising-edge of the clock. It also has an asynchronous reset. The counter also produces a carryout signal as shown in the figure below.



- iv) Write a test bench that generates a clock waveform of period 200 ns and 50% duty cycle (i.e. High for 100 ns and Low for 100 ns). Apply the following waveforms to a 4-bit counter instance.

Time	Reset	Enable
0	0	0
100	1	0
200	0	1
800	0	0
1200	0	1

