Unsigned Sequential Divider Design

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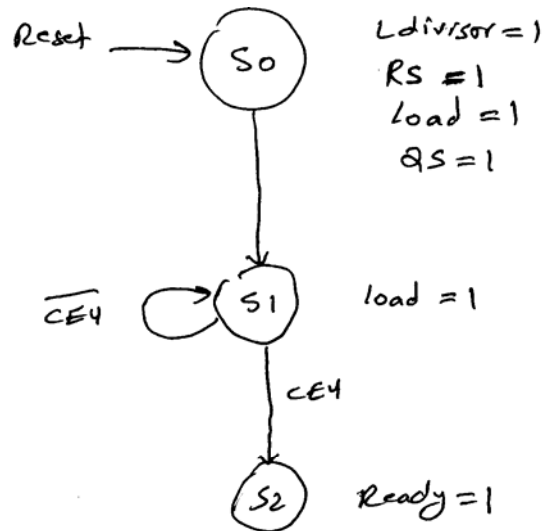
Datapath

Divisor

| Divisor | ← [AND gate] | LdNrsor
| | | clk

Rem [2:0], Quotient[3]

Cout

subtractor

Cout

| 0 | 1 |
2 x1 Mux

0

RS — | 1 | 0 |
2x1 Mux

Dividend

Quotient [2:0], Cout

QS — | 1 | 0 |
2x1 Mux

clk — [AND gate] → | Rem |
load —

clk — [AND gate] → | Quotient |
load —

3-bit counter

clk — | Q_2 | Q_1 | Q_0 | ← reset

CE4

Control Unit

Reset $\longrightarrow$ (S0)   Ldivisor = 1
                    RS = 1
                    load = 1
                    QS = 1

$\overline{CE4}$ ⟲ (S1)   load = 1

| CE4

(S2)   Ready = 1
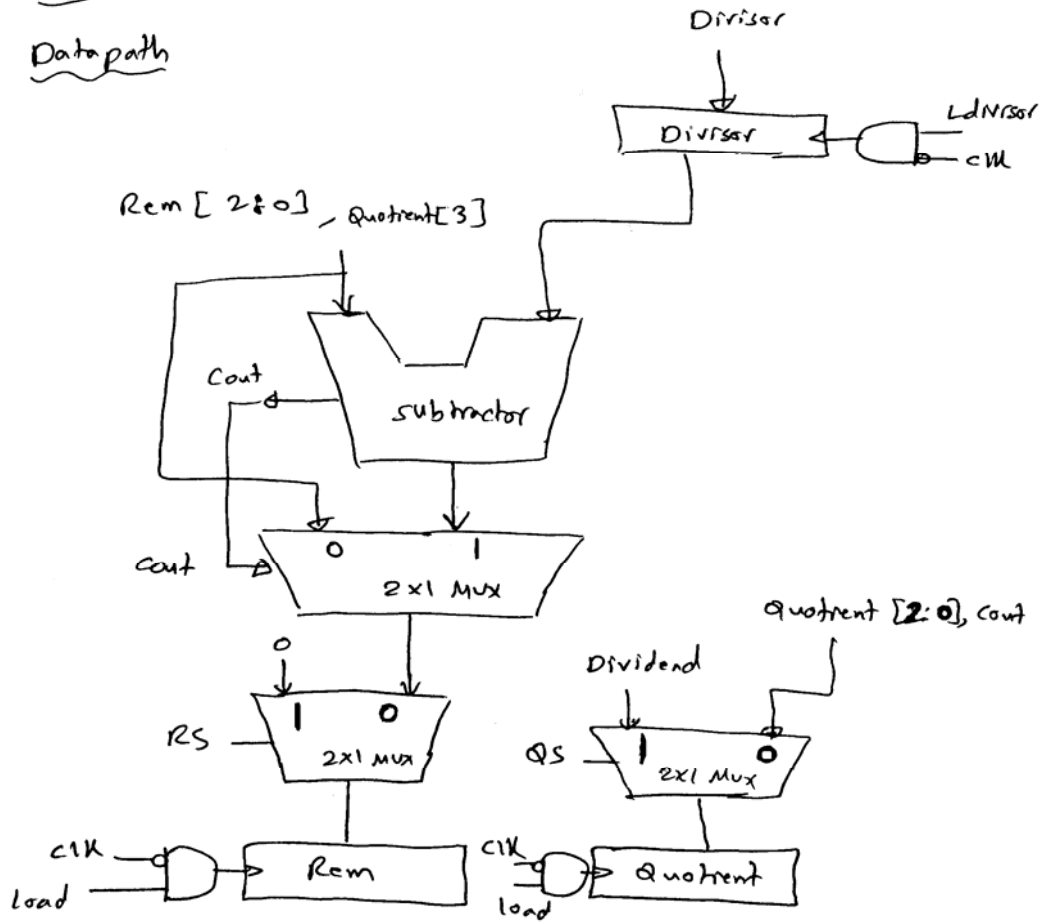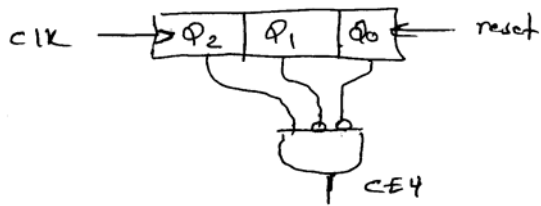
Recommended State assignment:

$$S0 = 11$$
$$S1 = 10$$
$$S2 = 01$$

To guarantee correct operation, reset
needs to be synchronous.