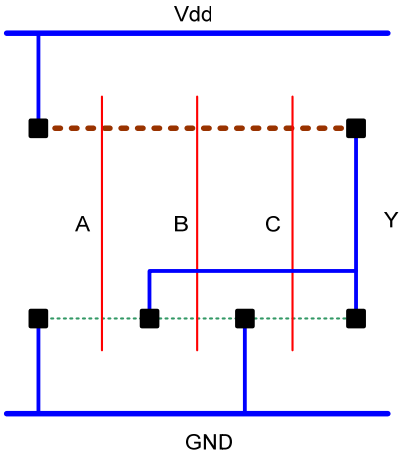
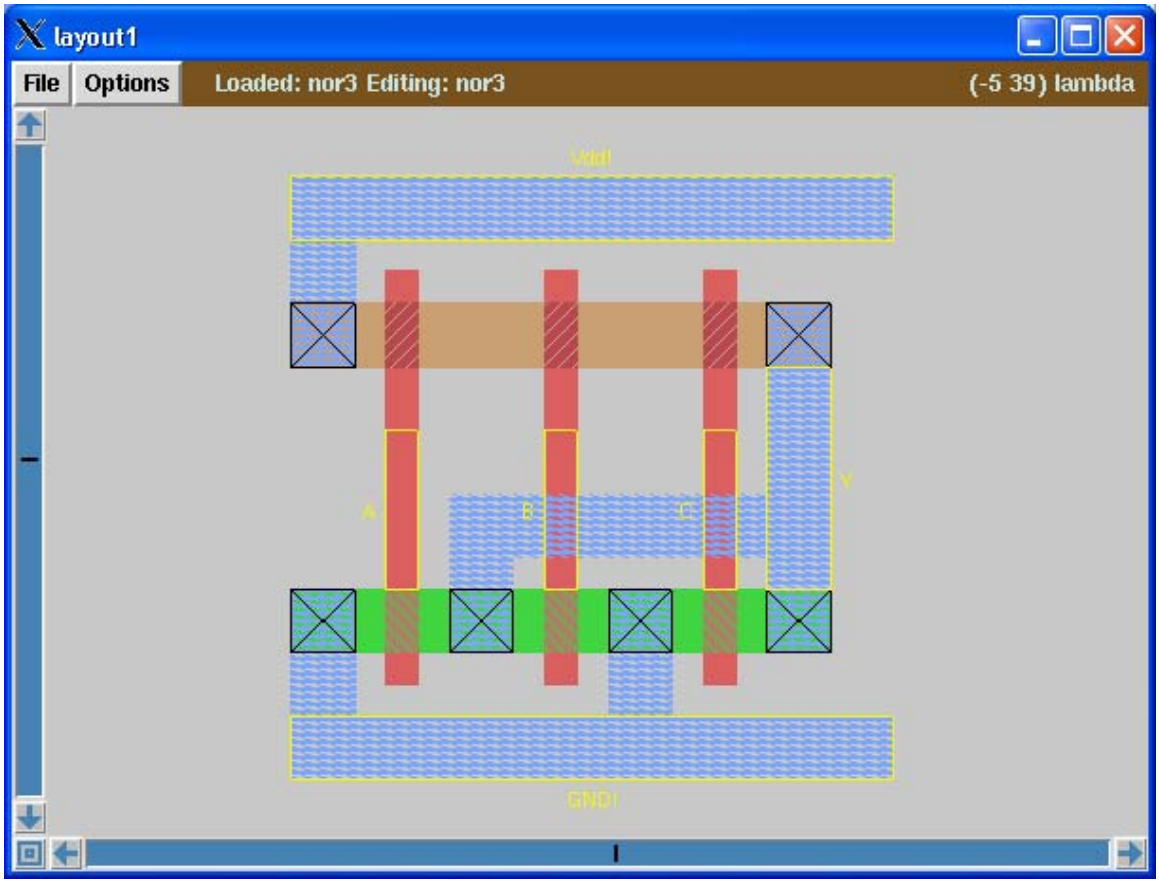
COE 360 **Dr. El-Maleh**

Quiz#6 Solution

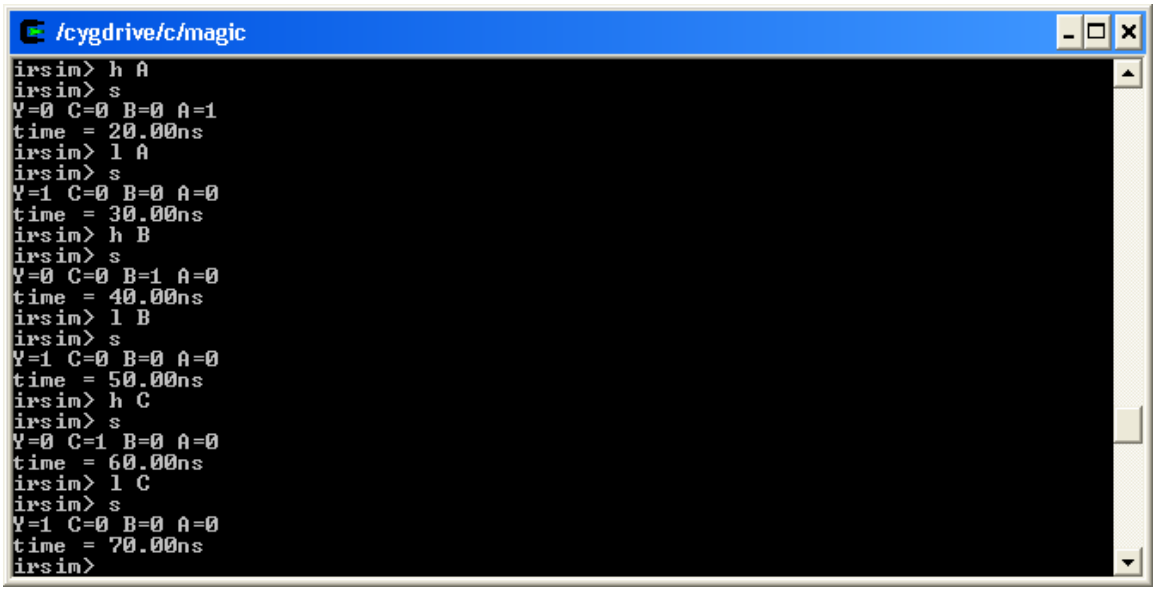
(i) Stick Diagram:



(ii) Magic Layout of the 3-input NOR gate:



(iii)&(iv) Functional Verification using IRSIM simulator:



(v) Extracted Spice Model:

```
* SPICE2 file created from nor3.ext - technology: scmos

M0 0 1 2 2 pfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M1 3 4 0 2 pfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M2 5 6 3 2 pfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M3 5 1 7 8 nfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M4 7 4 5 8 nfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M5 5 6 7 8 nfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
** GND == 7
** Y == 5
C0 5 GND 18.6fF
** a_n9_15# == 3
** a_n24_15# == 0
** Vdd == 2
C1 2 GND 19.5fF
** C == 6
C2 6 GND 8.9fF
** B == 4
C3 4 GND 8.9fF
** A == 1
C4 1 GND 8.9fF
** Gnd == 8
```

This file is modified to add the transistor models, specify Vdd and also to apply appropriate values on inputs. Note that if you get multiple Vdd and GND nodes, rename all of them such that you have one GND node and one Vdd node. Make sure that your GND node is numbered 0.

The spice file after modification is:

```
* SPICE2 file created from nor3.ext - technology: scmos

M0 8 1 2 2 pfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M1 3 4 8 2 pfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M2 5 6 3 2 pfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M3 5 1 0 0 nfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M4 0 4 5 0 nfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
M5 5 6 0 0 nfet w=6u l=3u
+ ad=0p pd=0u as=0p ps=0u
** GND == 0
** Y == 5
C0 5 0 18.6fF
** a_n9_15# == 3
** a_n24_15# == 0
** Vdd == 2
**C1 2 0 19.5fF
** C == 6
C2 6 0 8.9fF
** B == 4
C3 4 0 8.9fF
** A == 1
C4 1 0 8.9fF
** Gnd == 0



.Model nfet nmos (vto=0.8 lambda=0 gamma=0 cj=1.4e-4 cjsw=4.5e-10
+ld=0.1e-6 phi=0.6 tox=100e-9 rsh=3)
.Model pfet pmos (vto=-0.8 lambda=0 gamma=0 cj=5.6e-4 cjsw=7.1e-11
+ld=0.1e-6 phi=0.6 tox=100e-9 rsh=3)

Vdd 2 0 dc 5
vA 1 0 dc pulse (5.0 0.0 10ns 2ns 2ns 30ns 60ns)
vB 4 0 dc pulse (5.0 0.0 10ns 2ns 2ns 30ns 60ns)
vC 6 0 dc pulse (5.0 0.0 10ns 2ns 2ns 30ns 60ns)
*vA 1 0 dc 0
*vB 4 0 dc 0
*vC 6 0 dc 0

.tran 1ns 80ns
.plot tran v(1) v(5)
```

Below we will show the Tphl and Tplh for the specified conditions:

A	B	C	Y	Tphl
R	0	0	F	0.537ns
0	R	0	F	0.5ns
0	0	R	F	0.454ns
R	R	R	F	0.1ns

A	B	C	Y	Tplh
F	0	0	R	0.766ns
0	F	0	R	0.776ns
0	0	F	R	0.802ns
F	F	F	R	1.0647ns

Observations:

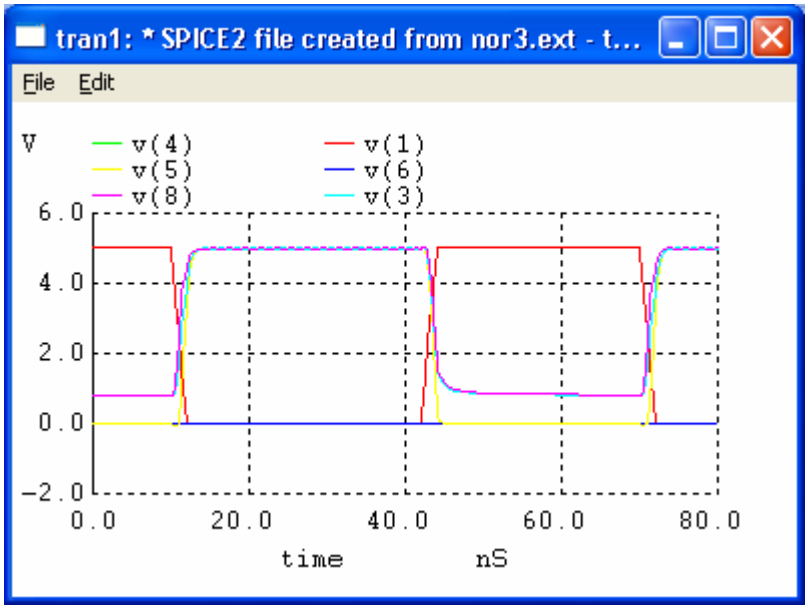
As can be seen from the tables above, the worst case Tphl is when input A is rising and the best case Tphl is when all the inputs are rising. This is because when input A is rising the three capacitors at node 8, 3, and 5 (the output) will discharge to 0. However, when input B is rising, only the two capacitors at nodes 3 and 5 will discharge leading to less delay. Similarly, when input C is rising, only the capacitor at node 5 will discharge leading to a less delay. When all the inputs are rising, only the capacitor at node 5 will discharge. The delay is less than that when the input C is changing although the same capacitor is discharged because the pull-down resistance is smaller as current flows across the three nmos transistors.

The worst case Tplh is found when all the inputs are falling and the best case is when only input A is falling. When input A is falling, once the A pmos transistor turns on, the capacitor at node 8 will start charging. The current flowing across the A pmos transistor will be more than that flowing across the B pmos transistor since the voltage difference across the A pmos transistor is higher. So, the net effect is that the capacitor at node 8 will be charging. The same argument applies for the other capacitors. So, all the three capacitors at nodes 8, 3, and 5 will be charging. However, when input B is falling, when the B pmos transistor turns on, the current flowing across the B pmos transistor will be more than that flowing across the A pmos transistor due to voltage difference. Thus, the net effect is that the capacitor at node 8 will be initially discharging while the capacitor at node 3 will be charging. The same applies for the capacitor at node 5, it will also be charging since the current flowing across it will be more that the current flowing out of it. Eventually, the capacitor at node 8 will be charging back. This is why this case has more delay than when A input is falling. When input C is falling, while the capacitor at node 5 will be charging both capacitors at nodes 8 and 3 will be discharging and eventually they will be charging back which makes the delay higher. Finally, when all the inputs are falling, while the capacitor at node 5 is charging, the capacitors at node 8 and 3 will be discharging and they will discharge more that the case when input C is falling due to the lower pull-down resistance and eventually they will be charging back. The delay in this

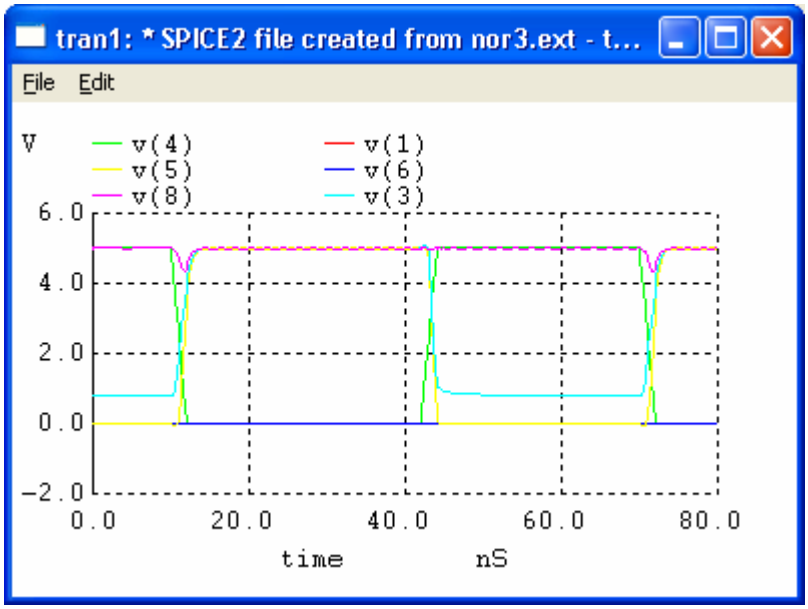
case is the highest because the capacitors at node 8 and 3 will discharge more so it will take more time to charge them back.

Below are the spice plots for the four cases:

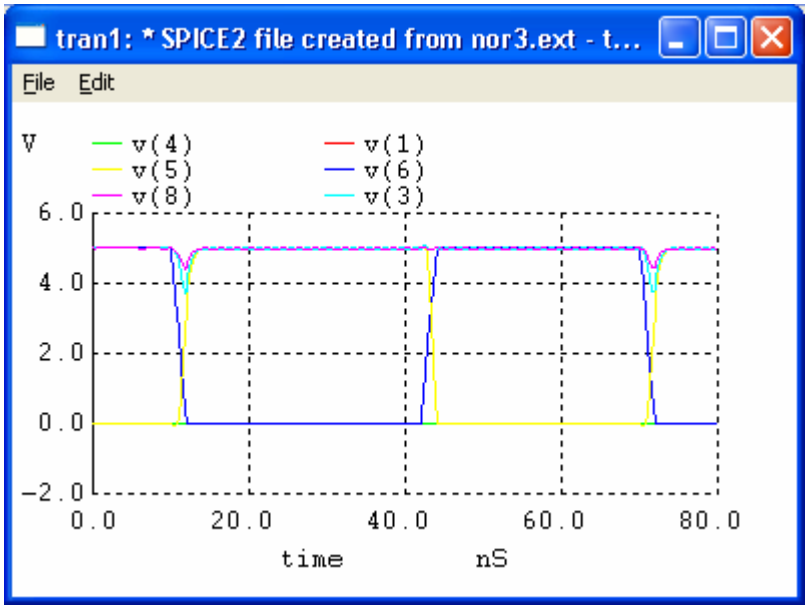
1. Input A is changing:



2. Input B is changing:



3. Input C is changing:



4. All inputs are changing: