Name: KEY **Id#**

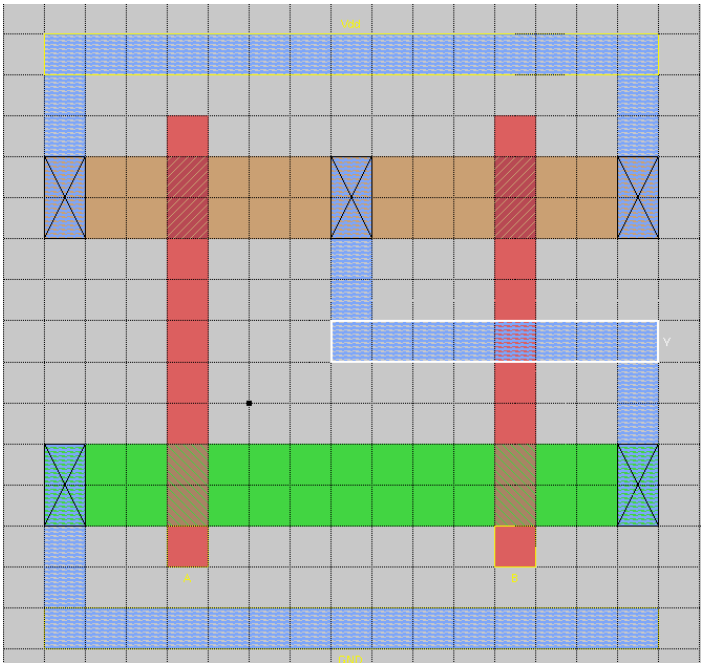
COE 360, Term 071

Principles of VLSI Design
Quiz# 5 (Take Home)

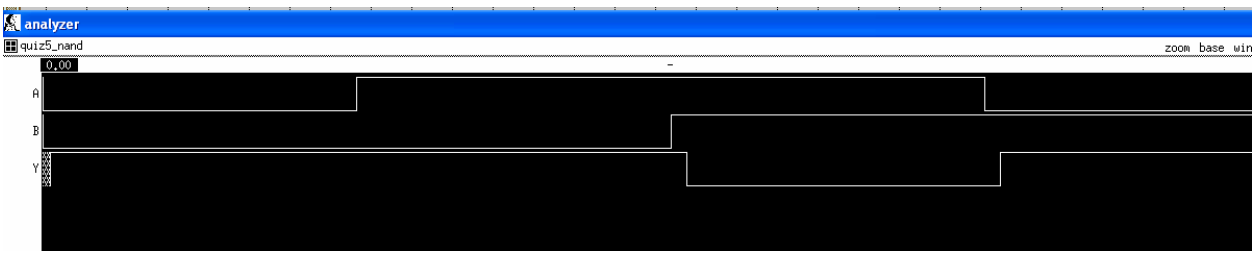
Due date: Saturday, Dec.1, 2007

Q1. You are required to draw the layout of a **2-input NAND** gate using magic. Use a grid size of 4 and make the length equal to 1 grid and the width equal to 2 grids for all nmos and pmos transistors.

(i) Include a snapshot of the drawn layout of the **2-input NAND** gate.



(ii) Extract a .sim model and verify that your model is working properly under all input combinations. Include a snapshot of your irsim simulation results.



(iii) Extract a spice model and add the required model statements and Vdd and verify that the circuit is working properly using spice. Include a snapshot of your spice simulation results.

Extracted Spice Model after necessary addition:

```
* SPICE3 file created from quiz5_nand.ext - technology: scmos

M0 Vdd A Y Vdd pfet w=8u l=4u
+ ad=0p pd=0u as=0p ps=0u
M1 Y B Vdd Vdd pfet w=8u l=4u
+ ad=0p pd=0u as=0p ps=0u
M2 a_n4_n12# A 0 0 nfet w=8u l=4u
+ ad=0p pd=0u as=0p ps=0u
M3 Y B a_n4_n12# 0 nfet w=8u l=4u
+ ad=0p pd=0u as=0p ps=0u
C0 0 0 14.3fF
C1 Vdd 0 14.3fF
C2 Y 0 18.8fF
C3 B 0 10.8fF
C4 A 0 10.8fF
.model nfet nmos (vto=1.0)
.model pfet pmos (vto=-1.0)
VDD vdd 0 DC 5
va A 0 dc pulse(0 5 10ns 0.5ns 0.5ns 20ns 40ns)
vb B 0 dc pulse(0 5 20ns 0.5ns 0.5ns 20ns 40ns)
.control
run
tran 0.01ns 60ns
plot v(A) v(B) v(Y)
.endc
.end
```

Spice Simulation: