Name: **Id#**

COE 360, Principles of VLSI Design, Term 981
Quiz# 5

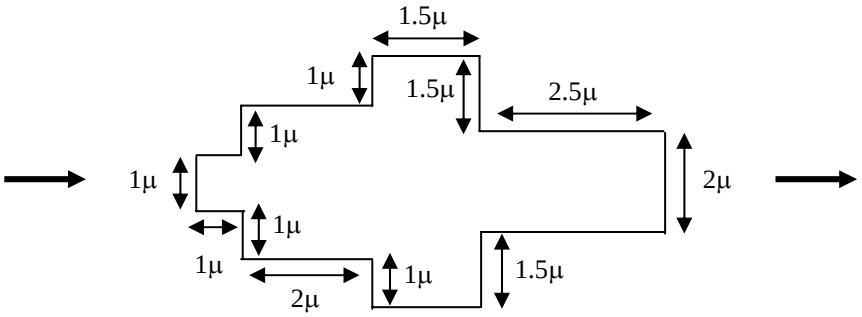
Date: Tuesday, June 18

(I) In a standard single metal N-Well CMOS fabrication process, the sheet resistance of various layers are given below:

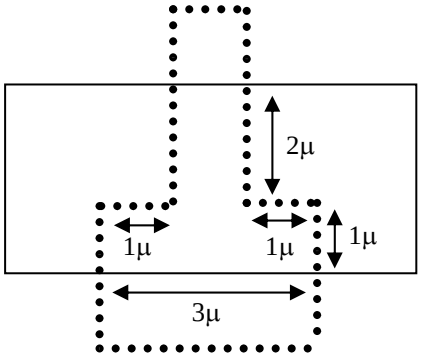
p-channel:	$15X10^3$	*Ω/SQ*
n-channel:	$6X10^3$	*Ω/SQ*
polysilicon:	20	*Ω/SQ*
n-diffusion:	40	*Ω/SQ*
p-diffusion:	150	*Ω/SQ*
Metal:	0.05	*Ω/SQ*

Since the current flow in corner squares is not uniform, it is assumed that the value of a corner square is equal to 0.66 the normal square resistance.

(i) Calculate the resistance of the following shapes for each of the polysilicon, n-diffusion, p-diffusion, and metal material types.



(ii) Calculate the p-channel resistance of the following transistor.



(II) Assume that for a CMOS inverter, the rising and falling times are given as 3.0 C_L/β_p, and 3.0 C_L/β_n, respectively.

(i) Design the circuit shown below such that the worst falling time is equal to 2ns, assuming that all dimensions of nmos and pmos transistors are equivalent.

(ii) Compute the best and worst rising times for the circuit.

(iii) What will be the dimensions of the pmos transistors to achieve a worst rising time equal to 2ns.

Assume C_L=0.1pF, $\mu_n C_{ox}$=100 uA/V^2, $\mu_p C_{ox}$=40 uA/V^2, and L=1um.