**Name:** **Id#**

**COE 360, Principles of VLSI Design, Term 981**
**Quiz# 5**

Date: Monday, Dec. 14

**(I)** A depletion-load inverter has an output low voltage $V_{OL}$ of 0.2V when $\beta_{load}/\beta_{driver}=0.18$. Assuming $(W/L)_{load}=1/3$, determine $(W/L)_A$, $(W/L)_B$, $(W/L)_C$, and $(W/L)_D$, for the circuit shown below such that the worst case $V_{OL}=0.2V$.

**(II)** Assume that for a CMOS inverter, the rising and falling times are given as 3.0 $C_L/\beta_p$, and 3.0 $C_L/\beta_n$, respectively.

**(i)** Design the circuit shown below such that the worst falling time is equal to 2ns, assuming that all dimensions of nmos and pmos transistors are equivalent.

**(ii)** Compute the best and worst rising times for the circuit.

**(iii)** What will be the dimensions of the pmos transistors to achieve a worst rising time equal to 2ns.

Assume $C_L$=0.1pF, $\mu_n C_{ox}$=100 uA/$V^2$, $\mu_p C_{ox}$=40 uA/$V^2$, and L=1um.