Name: **Id#**

COE 360, Term 071

Principles of VLSI Design
Quiz# 5 (Take Home)

Due date: Saturday, Dec.1, 2007

Q1. You are required to draw the layout of a **2-input NAND** gate using magic. Use a grid size of 4 and make the length equal to 1 grid and the width equal to 2 grids for all nmos and pmos transistors.

(i) Include a snapshot of the drawn layout of the **2-input NAND** gate.

(ii) Extract a .sim model and verify that your model is working properly under all input combinations. Include a snapshot of your irsim simulation results.

(iii) Extract a spice model and add the required model statements and Vdd and verify that the circuit is working properly using spice. Include a snapshot of your spice simulation results.