Name: **Id#**

COE 360, Principles of VLSI Design, Term 991
Quiz# 4

Date: Monday, Dec. 6

(Q.1.) Assume that for a CMOS inverter, the rising and falling times are given as 3.0 C_L/β_p, and 3.0 C_L/β_n, respectively.

(i) Design the circuit shown below such that the worst falling time is equal to 2ns and the circuit has Vth=2.5v when all the inputs switch simultaneously. Use the smallest possible dimensions for the transistors.

(ii) Compute the best and worst rising times for the circuit.

(iii) Compute the power that will be dissipated by the circuit, when the input values change from (A=0,B=0,C=0,D=1) to (A=1,B=1,C=0,D=1), assuming a frequency of 50 MHZ.

Assume that C_L=0.1pF, $\mu_n C_{ox}$=100 uA/V^2, $\mu_p C_{ox}$=40 uA/V^2, L=1um, Vtn=1v, and Vtp=-1v.