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COE 360, Principles of VLSI Design, Term 011
Quiz# 4

Date: Saturday, Dec. 1

(Q.1.) Assume that for a CMOS inverter, the propagation delays t_{PLH} and t_{PHL} are given as 0.7 C_L/β_p, and 0.7 C_L/β_n, respectively.

(i) Design a 2-inpu NAND gate such that the worst t_{PHL} time is equal to 1ns and Vth=2.5v, when all the inputs switch simultaneously. Use the smallest possible dimensions for the transistors.

(ii) Compute the best and worst t_{PLH} times for the 2-input NAND gate.

(iii) Compute the power dissipated by the 2-input NAND gate, when the input values change from (A=1,B=1) to (A=0,B=0), assuming a clock frequency of 200 MHZ.

(iv) Compute the power dissipated by the 2-input NAND gate, when the input values change from (A=0,B=1) to (A=1,B=1), assuming a clock frequency of 200 MHZ.

(v) Compute the average power dissipated by the 2-input NAND gate, assuming a clock frequency of 200 MHZ.

Assume that C_L=0.1pF, $\mu_n C_{ox}$=100 uA/V^2, $\mu_p C_{ox}$=40 uA/V^2, L=0.25um, Vdd=5v, Vtn=1v, and Vtp=-1v.