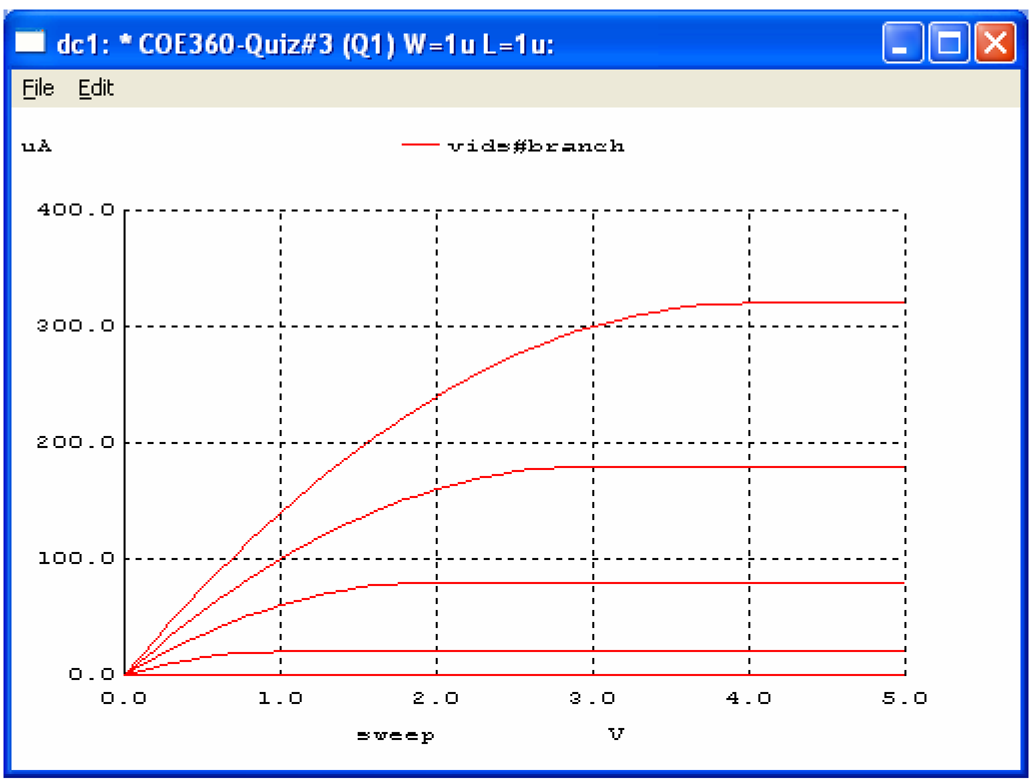
COE 360, Principles of VLSI Design, Term 032
Quiz# 3

Solution

Q1. Consider an nMOS transistor with a threshold voltage V_{tn}=1v, L=1u, and W=2u.

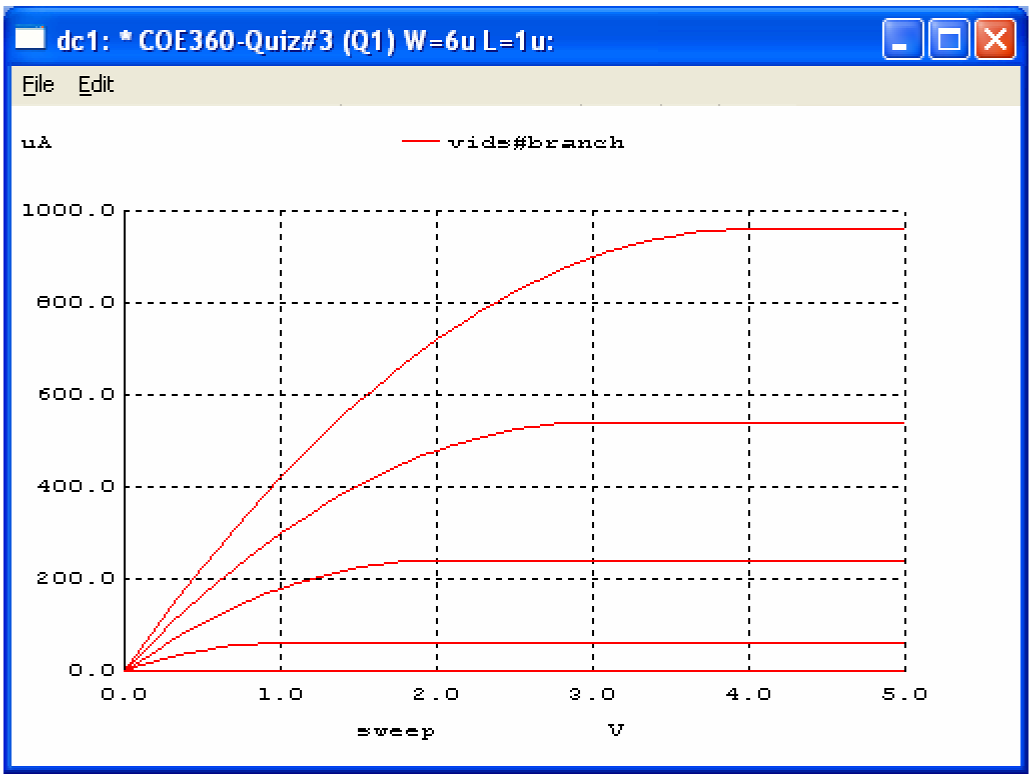
1. Using spice, draw the voltage-current graph by changing Vgs from 1v to 5v, and Vds from 0v to 5v.

```
* COE360-Quiz#3 (Q1) W=2u L=1u:
* Current-Voltage Characteristics of an NMOS transistor
m1 2 1 0 0 nfet W=2u L=1u
vgs  1 0 DC
vds  3 0 DC
vids 3 2
.model nfet nmos (vto=1.0)
.DC vds 0 5 0.1 vgs 1 5 1
.plot dc i(vids)
.end
```



2. Redraw the voltage-current graph by changing W to 6u. What are your observations?

```
* COE360-Quiz#3 (Q1) W=6u L=1u:
* Current-Voltage Characteristics of an NMOS transistor
m1 2 1 0 0 nfet W=6u L=1u
vgs  1 0 DC
vds  3 0 DC
vids 3 2
.model nfet nmos (vto=1.0)
.DC vds 0 5 0.1 vgs 1 5 1
.plot dc i(vids)
.end
```



As we can see, the current is directly related to the width of the transistor. By increasing W by 3 times, the current increases by 3 times.

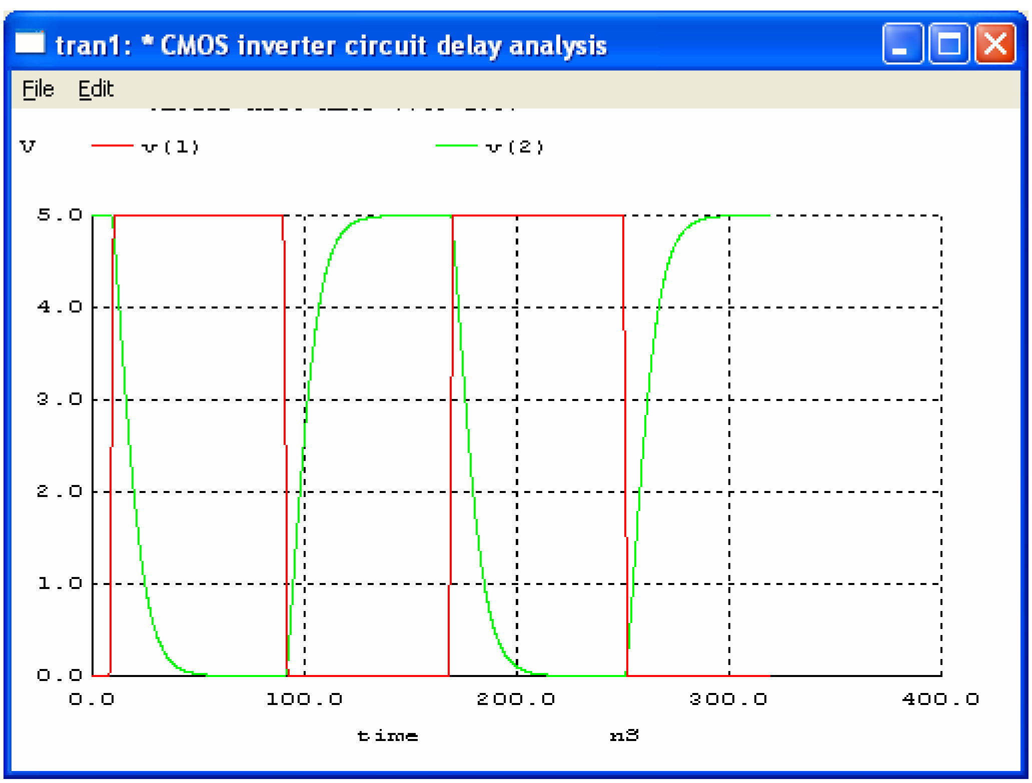
Q2. Model a CMOS inverter using SPICE. Assume that the threshold voltage for the nmos transistor is 1v and that of the pmos transistor is -1v. Do not specify the other parameters so that the default parameters are used. Use a length of 1u and a width of 2u for both the nmos and pmos transistors. Assume that the inverter has a load capacitance of 1pf.

1. Define a pulse on the input of the inverter that changes from 0 to 5 volts after 8ns, it has a rising time of 2ns and a falling time of 2 ns. The pulse stays at 5 volts for 80 ns and the period of the pulse is 160ns.

2. Perform a transient analysis for 320ns and plot the input and the output of the CMOS inverter.

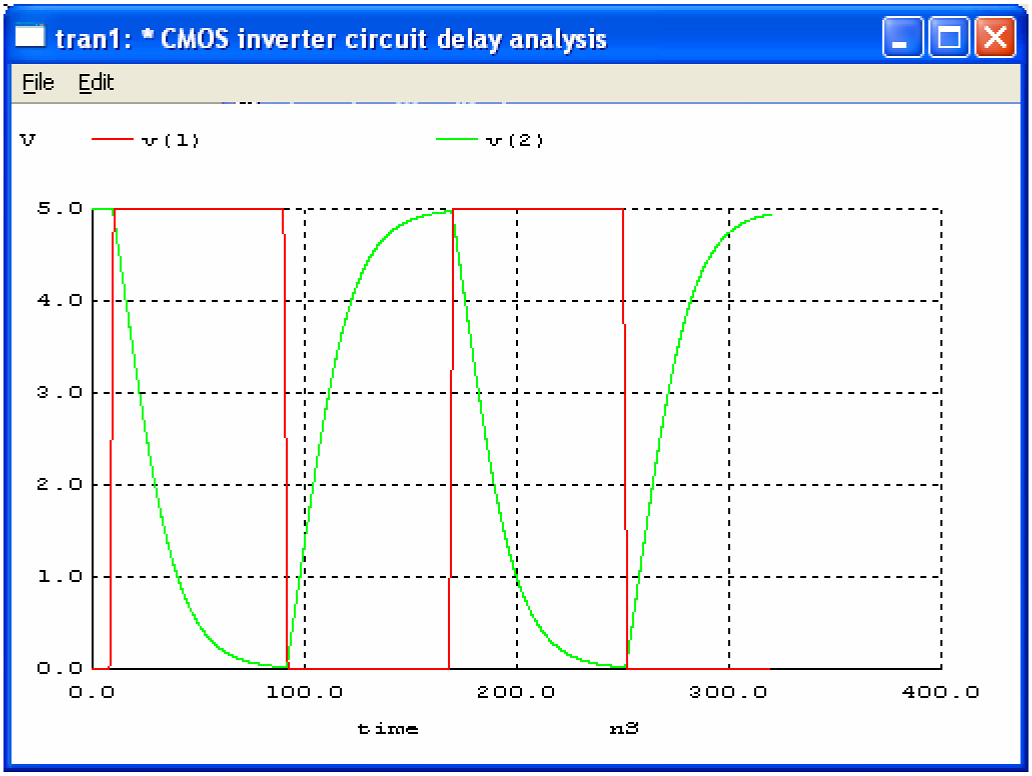
```
* CMOS inverter circuit delay analysis
m1 2 1 0 0 nfet W=2u L=1u
m2 2 1 3 3 pfet W=2u L=1u
c1 2 0 1p
vdd 3 0 dc 5.0
vin 1 0 dc pulse (0.0 5.0 8ns 2ns 2ns 80ns 160ns)
.model nfet nmos (vto=1.0)
.model pfet pmos (vto=-1.0)
.tran 0.1ns 320ns
.plot tran v(1) v(2)
.end
```

3. Compute the propagation delays t_{PLH} and t_{PHL} for this CMOS inverter.



t_{PLH} = 17.5 – 9 = 8.5 ns
t_{PHL} = 99.52 – 91 = 8.52 ns

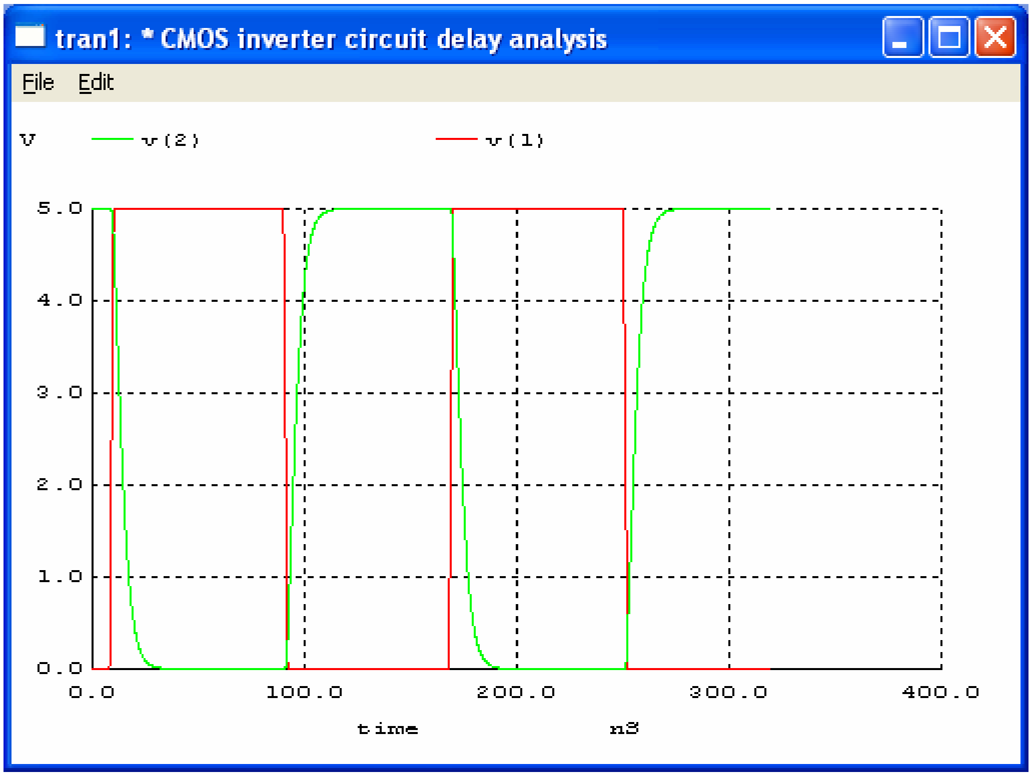
4. Change the load capacitor from 1 pf to 2 pf and recompute the propagation delays t_{PLH} and t_{PHL} for this CMOS inverter. What are your observations?



t_{PLH} = 25.57 – 9 = 16.57 ns
t_{PHL} = 107.45 – 91 = 16.45ns

As can be seen, by doubling the size of the load capacitor, the delay almost doubles. This is because the delay is related to the load capacitance of the inverter. The reason that it does not exactly doubles is because the capacitance of the inverter is calculated based on the load capacitor and the patristic capacitances extracted from the transistors.

5. Change the width of the nmos and pmos transistors to 4u and using a load capacitor of 1 pf, recompute the propagation delays t_{PLH} and t_{PHL} for this CMOS inverter. What are your observations?



t_{PLH} = 13.496 – 9 = 4.496 ns
t_{PHL} = 95.494. – 91 = 4.494ns

As can be seen, by increasing the width of transistors from 2u to 4u we are reducing their resistance by half, so the delay should decrease by half. However, since the patristic capacitances increase by increasing the dimensions of the transistors, the delay is not reduced exactly by half.