Name: **Id#**

COE 360, Principles of VLSI Design, Term 991
Quiz# 3

Date: Saturday, Nov. 6

Q1. Indicate whether the following is true or false, and if it is false indicate why it is false:

(1) (True, False) Guard rings are used for latchup prevention since they increase the values of R_{sub} and R_{well}.

(2) (True, False) Latchup takes place if the voltage I R_{sub} or I R_{well}, resulting from induced current I, is large enough to forward-bias the base-emitter junction of one of the parasitic transistors.

(3) (True, False) To ensure low threshold voltage of parasitic MOS transistors existing between unrelated transistors, we need to have thick field oxide and raise impurity concentration in the substrate by introducing channel-stop diffusion.

(4) (True, False) Following the growth of a thin gate oxide on top of the active regions, a set of two masks are used to implant the n+ and p+ regions into the substrate and into the n-well, respectively.

(5) (True, False) The polysilicon layer is deposited over the entire active regions to define the gate electrodes of the nmos and pmos transistors.

(6) (True, False) A metal2 layer can be connected to polysilicon layer through a contact hole called VIA.

(7) (True, False) Following layout design rules guarantees successful chip fabrication and results in functional chips.

Q2. Draw the stick diagram layout of the transistor-level implementation shown below. Minimize the wire lengths and the contact cuts used.