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COE 360, Term 071

Principles of VLSI Design
Quiz# 3 (Take Home)

Due date: Saturday, Nov.17, 2007

Q1. Model a **2-input CMOS NAND gate**, $Y=(A \cdot B)'$, using SPICE. Assume that the threshold voltage for the nmos transistor is 1 V and that of the pmos transistor is -1 V. Do not specify the other parameters so that the default parameters are used. Use a length of 1u and a width of 2u for both the nmos and pmos transistors. Assume that the NAND gate has a load capacitance of 1pf.

1. Verify that your model correctly performs the behavior of a 2-input NAND gate by showing the output for all the possible input combinations on the two inputs.
2. Define a pulse on the **A** input of the inverter that changes from 0 to 5 volts after 10ns, it has a rising time of 3ns and a falling time of 3 ns. The pulse stays at 5 volts for 120 ns and the period of the pulse is 246ns. Keep the **B** input constant to 1.
3. Perform a transient analysis for 300ns and plot the input and the output of the CMOS NAND gate.
4. Compute the propagation delays t_{PLH} and t_{PHL} for this CMOS NAND gate under this condition of changing the **A** input while keeping the **B** input constant to 1.
5. Repeat steps 2-4 by defining the pulse on the **B** input while keeping the **A** input connected to 1. Compute the propagation delays t_{PLH} and t_{PHL} and compare to what you got in 4. Comment on your observations.
6. Change the load capacitor from 1 pf to 2 pf and recompute the propagation delays t_{PLH} and t_{PHL} for this CMOS NAND gate when the **A** input is changing. Comment on your observations.
7. Change the width of the nmos and pmos transistors to 4u and using a load capacitor of 1 pf, recompute the propagation delays t_{PLH} and t_{PHL} for this CMOS NAND gate when the **A** input is changing. What are your observations?

Q2. Model a **2-input CMOS XOR gate**, $Y=(A \oplus B)$ using only NAND gates. The NAND gates should be instantiated as subcircuits. Assume that the XOR gate has a load capacitance of 1pf. Verify that your model correctly performs the behavior of a 2-input XOR gate by showing the output for all the possible input combinations on the two inputs.