Name: **Id#**

COE 360, Principles of VLSI Design, Term 032
Quiz# 3

(Take Home)

Due date: Sunday, March 28, 2004

Q1. Consider an nMOS transistor with a threshold voltage V_{tn}=1v, L=1u, and W=2u.

1. Using spice, draw the voltage-current graph by changing Vgs from 1v to 5v, and Vds from 0v to 5v.

2. Redraw the voltage-current graph by changing W to 6u. What are your observations?

Q2. Model a CMOS inverter using SPICE. Assume that the threshold voltage for the nmos transistor is 1v and that of the pmos transistor is -1v. Do not specify the other parameters so that the default parameters are used. Use a length of 1u and a width of 2u for both the nmos and pmos transistors. Assume that the inverter has a load capacitance of 1pf.

1. Define a pulse on the input of the inverter that changes from 0 to 5 volts after 8ns, it has a rising time of 2ns and a falling time of 2 ns. The pulse stays at 5 volts for 80 ns and the period of the pulse is 160ns.

2. Perform a transient analysis for 320ns and plot the input and the output of the CMOS inverter.

3. Compute the propagation delays t_{PLH} and t_{PHL} for this CMOS inverter.

4. Change the load capacitor from 1 pf to 2 pf and recompute the propagation delays t_{PLH} and t_{PHL} for this CMOS inverter. What are your observations?

5. Change the width of the nmos and pmos transistors to 4u and using a load capacitor of 1 pf, recompute the propagation delays t_{PLH} and t_{PHL} for this CMOS inverter. What are your observations?