COE 360, Principles of VLSI Design, Term 991
Course Project

4-bit Comparator

Due date: Saturday, December 11

It is required to design a 4-bit comparator using CMOS technology. The comparator gets two 4-bit numbers $A=A_3A_2A_1A_0$ and $B=B_3B_2B_1B_0$, and produces two outputs GT and LT. If A>B, then the output signal GT is set to 1, and if A<B, then the output signal LT is set to 1, otherwise both signals will be set to 0, which indicates that the two numbers are equal (i.e. A=B). The 4-bit comparator circuit can be designed in a modular way as shown below.

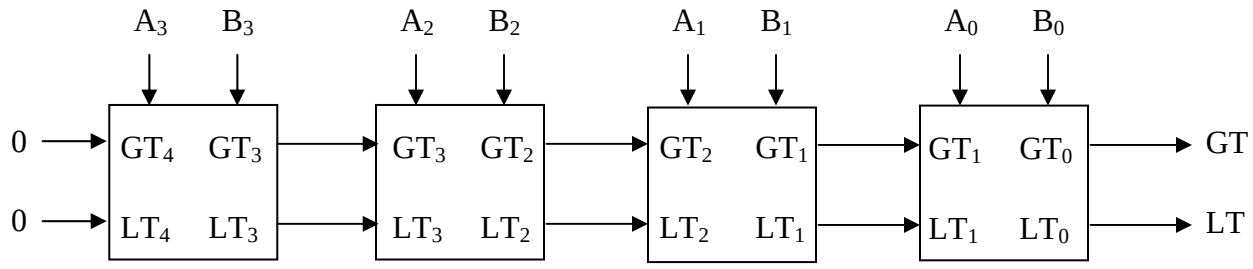

Figure 1 4-bit comparator - block diagram

The truth table and general arrangement for a binary 1-bit comparator bit-slice is shown below where A_i and B_i are the two bits to be compared, GT_{i+1} and LT_{i+1} are the inputs from outputs of the previous stage and GT_i and LT_i are the outputs of the current stage. If $A_i > B_i$, then $GT_i = 1$, and if $A_i < B_i$, then $LT_i = 1$. Both GT_i and LT_i will be equal to 0 if $A_i = B_i$.

Inputs				Outputs	
A_i	B_i	GT_{i+1}	LT_{i+1}	GT_i	LT_i
X	X	1	0	1	0
X	X	0	1	0	1
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	0	1	0
1	1	0	0	0	0

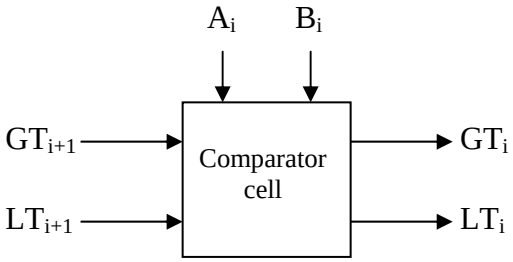

Figure 2 Comparator cell behavior

To complete the project, you need to do the following steps:

1. Design the gate-level and the transistor-level schematic of the basic cell of 1-bit comparator.

2. Draw the stick diagram layout of the basic cell of 1-bit comparator.

3. Using MAGIC, draw the initial layout of the basic cell of 1-bit comparator having all nMOS transistors with a (W/L) ratio of 1, and all pMOS transistors with a (W/L) ratio of 2. Assume that the minimum feature size is used for all transistors.

4. Extract the transistor-level circuit from the layout of the basic cell, using the command ***extract***, convert it into the simulator format, using ***ext2sim***, and then simulate it using ***irsim*** and verify that it is working properly for all input combinations.

5. Extract the SPICE model of the basic comparator cell, using the command ***ext2spice***. Then, using SPICE, determine the maximum propagation delay across the cell. You need to use the following models for the **nfet** and **pfet** transistors:

.Model nfet nmos (vto=0.8 lambda=0 gamma=0 cj=1.4e-4 cjsw=4.5e-10 ld=0.1e-6 phi=0.6 tox=100e-9 rsh=3)
.Model pfet pmos (vto=-0.8 lambda=0 gamma=0 cj=5.6e-4 cjsw=7.1e-11 ld=0.1e-6 phi=0.6 tox=100e-9 rsh=3)

6. Draw the layout of the 4-bit comparator circuit based on its basic cell using the ***array*** command. Then, simulate it using ***irsim*** to verify that it is working properly.

7. Deduce the maximum propagation delay of the 4-bit comparator based on the maximum delay across one cell. Then, extract the SPICE model of the 4-bit comparator and determine the maximum propagation delay across it. Compare your estimated delay to what you found based on spice and comment about it.

11. Using the **power-meter** technique, determine the maximum power dissipated by the basic comparator cell. Then, determine the maximum power dissipated by the 4-bit comparator. Comment on your observations.

12. Optimize the speed of the 4-bit comparator circuit by resizing the transistors width and length to reduce the maximum propagation delay of the initial design by 50%. Change your spice model based on the new transistor sizes and verify it. (Note: You do not need to redraw the layout for this part.)

13. Right a report describing your design. The report should include the following:

- Gate-level schematic for the basic comparator cell.
- Transistor-level schematic for the basic comparator cell.
- Stick-diagram layout for the basic comparator cell.
- Layout printout for the basic comparator cell and for the 4-bit comparator.

- Irsim simulation printouts indicating that the basic comparator cell and the 4-bit comparator are working properly.
- Spice simulation printouts indicating the maximum propagation delay across the basic comparator cell and the 4-bit comparator for the initial design.
- Spice simulation printouts indicating the maximum propagation delay across the basic comparator cell and the 4-bit comparator for the optimized design.

- Spice simulation printouts indicating the maximum power dissipation, using the power-meter technique, across the basic comparator cell and the 4-bit comparator for the initial design.

The project is to be conducted by a group of a maximum of three students. Area optimization and neatness of the layout design will be evaluated. Organization and completeness of the report is important.