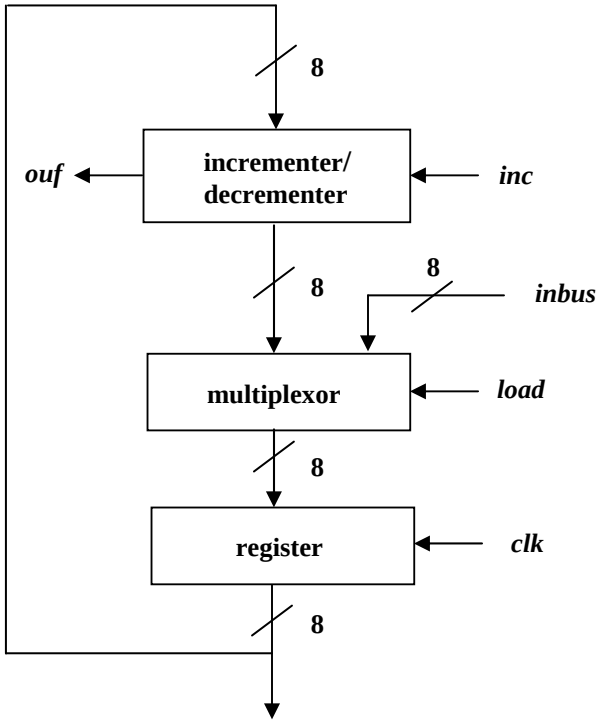
COE 360, Principles of VLSI Design, Term 982
Course Project

Due date: Saturday, May 15

It is required to design an 8-bit loadable up/down counter using CMOS technology. The block diagram of the counter is shown below. It consists of three main components namely, an incrementer/decrementer, a multiplexor, and a register. The signal ***inc*** indicates whether the counter should be counting upward or downward. When ***inc*** is set to 0 the counter counts up otherwise it counts down. The counter indicates when it reaches either an overflow or underflow condition by setting the output signal ***ouf*** to 1. When the signal ***load*** is set to 1, the counter is loaded with the value provided in the 8-bit input ***inbus***. The counter has a rising-edge synchronizing clock signal ***clk***.



To complete the project, you need to do the following steps:

1. Design the top-level 8-bit loadable up/down counter as consisting of three main components, namely, an 8-bit incrementer/decrementer, an 8-bit 2X1 multiplexor, and an 8-bit rising-edge triggered register.

2. Design each of the three components using a modular design approach, i.e., a basic cell is designed that can be replicated 8 times to get an 8-bit component.

3. Draw the gate-level and the transistor-level schematic of the basic cell of each component.

4. Draw the stick diagram layout of the basic cell of each component.

5. Using MAGIC, draw the initial layout of the basic cell of each component having all nMOS transistors with a (W/L) ratio of 1, and all pMOS transistors with a (W/L) ratio of 2. Assume that the minimum feature size is used for all transistors.

6. Compact the layout of each cell of the basic components using the ***plow*** command, to optimize the used area.

7. Extract the transistor-level circuit from the layout of each basic cell, using the command ***extract***, convert it into the simulator format, using ***ext2sim***, and then simulate it using ***irsim*** and verify that it is working properly for all input combinations.

8. Extract the SPICE model of the basic cell from each component, using the command ***ext2spice***. Then, using SPICE, determine the maximum propagation delay across each cell. Deduce the maximum propagation delay across each component. You need to use the following models for the **nfet** and **pfet** transistors:

.Model nfet nmos (vto=0.8 lambda=0 gamma=0 cj=1.4e-4 cjsw=4.5e-10 ld=0.1e-6 phi=0.6 tox=100e-9 rsh=3)
.Model pfet pmos (vto=-0.8 lambda=0 gamma=0 cj=5.6e-4 cjsw=7.1e-11 ld=0.1e-6 phi=0.6 tox=100e-9 rsh=3)

9. Draw the layout of each component based on its basic cell using the ***array*** command. Simulate each component using ***irsim*** to verify that it is working properly.

10. Connect the layout of all components to complete the 8-bit loadable up/down counter layout. Then, simulate the design using ***irsim*** and verify that it is working properly.

11. Extract the SPICE model of each component and determine the maximum frequency under which each operates properly.

12. Extract the SPICE model of the 8-bit up/down counter and determine the maximum frequency under which it operates properly.

13. Using the **power-meter** technique, determine the maximum power dissipated by the 8-bit up/down counter.

14. Right a report describing your design. The report should include the following:

- Modular block diagram for each of the three main components.
- Gate-level schematic for basic cell of each component.
- Transistor-level schematic for basic cell of each component.
- Stick-diagram layout for basic cell of each component.

- Layout printout for basic cell of each component.
- Layout printout for each of the three main components.
- Layout printout for the whole 8-bit loadable up/down counter.
- Irsim simulation printouts indicating that the basic cell of each component is working properly.
- Irsim simulation printouts indicating that each component is working properly.
- Irsim simulation printouts indicating that the whole 8-bit loadable up/down counter is working properly.
- Spice simulation printouts indicating the maximum propagation delay across each basic cell.
- Spice simulation printouts indicating the maximum propagation delay across each component.

- Spice simulation printouts indicating the maximum propagation delay across the 8-bit up/down counter.

- Spice simulation printouts indicating the maximum power dissipation, using the power-meter technique, across the 8-bit up/down counter.

The project is to be conducted by a group of two students. Organization and completeness of the report is important.