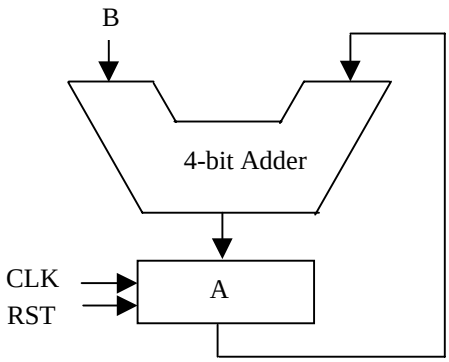
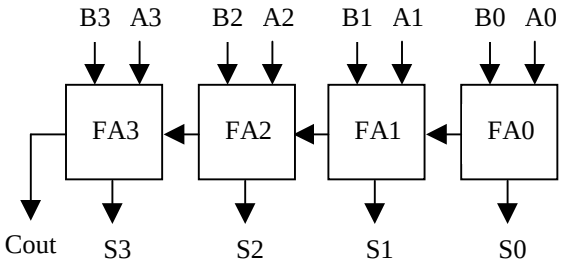
COE 360, Principles of VLSI Design, Term 981
Course Project

Due date: Monday December 9

It is required to design a 4-bit accumulator circuit using CMOS technology. The accumulator circuit shown below is designed using a 4-bit register with a synchronous rising-edge clock, CLK, and asynchronous reset, RST. When RST=0, the accumulator is reset to 0 asynchronously.



The adder used in the design of the accumulator is a 4-bit ripple-carry adder, as shown below. Assume that the carry out signal of the adder will be stored in a status register.



In this project, you are required to design the 4-bit ripple-carry adder using CMOS technology such that it works for a frequency of 50MHZ.

To complete the project, you need to do the following steps:

1. Draw the gate-level schematic of the one-bit full-adder circuit. You can consider the full-adder circuit as one cell producing the sum and the carry-out signals or as two separate cells, one for the sum and the other for the carry out.

2. Draw the transistor-level schematic of the one-bit full-adder circuit.

3. Draw the stick diagram layout of the one-bit full adder circuit.

4. Using MAGIC, draw the initial layout of the one-bit full adder circuit having all nMOS transistors with a (W/L) ratio of 2, and all pMOS transistors with a (W/L) ratio of 4. Assume that the minimum feature size is used for all transistors.

5. Extract the one-bit full-adder circuit from your layout, using the command ***extract***, convert it into the simulator format, using ***ext2sim***, and then simulate it using ***irsim*** and verify that it is working properly for all input combinations.

6. Extract the SPICE model of the one-bit full-adder circuit, using the command ***ext2spice***. Then, using SPICE, determine the transition and propagation delay times of the sum and carry-out signals.

7. If your design does not meet the required constraints, then change your layout by modifying the (W/L) ratios of the transistors. Determine the required (W/L) ratios by analysis of your design. Modify your layout and verify using SPICE simulation that it satisfies the performance requirement.

8. Compact your full-adder circuit, using the ***plow*** command, to optimize the used area.

9. Define your 4-bit adder as a cell containing 4 instances of the one-bit full-adder cell. Draw the layout of the 4-bit adder using the ***array*** command.

10. Connect the 4 full-adder cells together to complete the 4-bit adder circuit layout. Then, simulate the 4-bit adder using ***irsim*** and verify that it is working properly. Verify that it is working properly for the following input combinations:

A	B

0000	**1111**
1111	**0000**
0101	**1010**
1111	**1111**
0101	**0101**
0011	**1101**
0111	**0001**
0001	**1111**

11. Extract the SPICE model of the 4-bit adder and determine the maximum propagation delay of the adder. Determine the maximum frequency under which the adder will work properly.

12. Determine the maximum power dissipated by the 4-bit adder.

[13-15 Optional: Additional 5% of your grade bonus]

13. Draw the transistor-level schematic of a rising-edge DFF with asynchronous reset.

14. Draw the stick diagram layout of the DFF.

15. Draw the layout of the DFF using MAGIC and simulate it using ***irsim*** to verify that it is working properly. Then, construct the layout of a 4-bit register using the DFF layout. Finally, draw the layout of the 4-bit accumulator using the layout of the 4-bit adder and the layout of the 4-bit register. Verify that the whole design is working properly using ***irsim***. Simulate a 4-bit counter using the designed accumulator.

All layout plots, circuit diagrams, and SPICE simulation results on speed and power should be submitted with a final report by the end of the project deadline. Organization and completeness of the report is important.