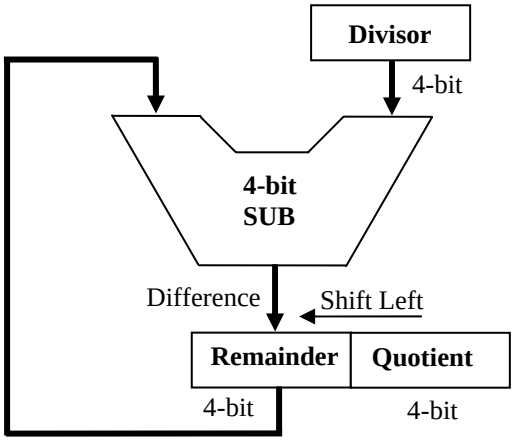
COE 360, Principles of VLSI Design, Term 071
Course Project

Unsigned Sequential Divider

It is required to design an 4-bit unsigned divider using CMOS technology. The divider divides an 4-bit dividend number, A, by an 4-bit divisor number, B. It produces an 4-bit quotient and an 4-bit remainder. Assume that the divider will be a sequential divider and it will set the signal Ready to 1 when the quotient and remainder results are ready. The divider has an asynchronous reset after which in the next clock cycle it starts the division process. The quotient and remainder will maintain their values unless the divider is reset again.

Part of the Datapath of the divider is given below:



The algorithm for performing sequential division is as follows:

1. Set Quotient=Dividend, Set Remainder=0.
2. Shift(Remainder, Quotient) Left by 1 bit
3. Difference=Remainder-Divisor
4. If (Difference≥ 0) Then
   Remainder=Difference
   Set Least Significant bit of Quotient to 1.
   End If;
5. If (#iterations<4) Then Goto Step 2.

An example of applying the algorithm for a 4-bit divider with dividend=1110 and divisor=0011 is given below. Note that the Quotient=0100 and the Remainder=0010.

Iteration		Remainder	Quotient	Divisor	Difference
0	Initialize	0 0 0 0	1 1 1 0	0 0 1 1	
1	1: SLL, Difference	0 0 0 1 ←	1 1 0 0	0 0 1 1	1 1 1 0
	2: Diff < 0 => Do Nothing				
2	1: SLL, Difference	0 0 1 1 ←	1 0 0 0	0 0 1 1	0 0 0 0
	2: Rem = Diff, set lsb Quotient	0 0 0 0	1 0 0 1		
3	1: SLL, Difference	0 0 0 1 ←	0 0 1 0	0 0 1 1	1 1 1 0
	2: Diff < 0 => Do Nothing				
4	1: SLL, Difference	0 0 1 0 ←	0 1 0 0	0 0 1 1	1 1 1 1
	2: Diff < 0 => Do Nothing				

To complete the project, you need to do the following step:

1. Derive the logic-level implementation of the 4-bit unsigned divider unit. Show the design of the datapth and control unit and their interaction.

2. Model your design using schematic capture (e.g. logic works or xilinix) and verify by simulation the correct operation of your design.

3. Derive the transistor-level implementation of the 4-bit unsigned divider unit.

4. Model the transistor-level implementation of the 4-bit unsigned divider unit using SPICE and verify its correct functionality.

5. Determine the **worst case propagation delay** across the subtractor unit and control logic. For the registers, determine the **setup** and **hold** time and the **FF propagation delay.** Assume that all nMOS transistors have a (W/L) ratio of 2, and all pMOS transistors have a (W/L) ratio of 4. Estimate the maximum frequency across which your design should work. Verify by spice simulations that your design works at the estimated maximum frequency. Comment on any discrepancies. Assume a load capacitor of 0.1 pF at the D-input of the FF and a 0.1 pF at the Q output of the D-FF.

6. Draw the stick diagram layout of your the 4-bit unsigned divider unit.

7. Using MAGIC, draw the layout of y the 4-bit unsigned divider unit assuming that all nMOS transistors are with a (W/L) ratio of 2, and all pMOS transistors are with a (W/L) ratio of 4. Assume that the minimum feature size is used for all transistors.

8. Extract the 4-bit unsigned divider unit from your layout, using the command ***extract***, convert it into the simulator format, using ***ext2sim***, and then simulate it using ***irsim*** and verify that it is working properly.

9. Extract the SPICE model of the 4-bit unsigned divider unit using the command ***ext2spice***. Then, using SPICE, determine the worst-case propagation delay times of the 4-bit unsigned

divider unit.

10. Write a professional report documenting all the design stages of the 4-bit unsigned divider unit. All layout plots, circuit diagrams, logic simulations, irsim simulations and SPICE simulation results should be submitted with a final report by the end of the project deadline. Organization and completeness of the report is important.

When extracting your design from Magic, extract it without extracting resistance and capacitances. Add a 0.1 pF on the D and Q inputs of the D-FF. You can do this by running the following sequence of commands from inside magic:
:Extract no resistance
:Extract no capacitance
:Extract

For SPICE simulations, Use the AMI 0.5U, 5V technology file posted in WebCT.

This project is to be carried out by a team of **three students**. Divide the project into components and distribute it among the team members. Each student is supposed to work on one component of the design. Report on team work activity in the report as this part will be evaluated.

The distribution of the project marks is as follows:

Task	**Mark**
Logic design of the 4-bit unsigned divider unit	**10%**
Verification of logic design by simulation	**10%**
Transistor-level design of the 4-bit unsigned divider unit	**10%**
Spice Simulation of transistor-level design and timing analysis	**15%**
Stick diagram layout of the 4-bit unsigned divider unit	**10%**
Magic layout of the 4-bit unsigned divider unit	**20%**
Logic verification of the extracted 4-bit unsigned divider unit using Irsim	**10%**
Spice simulation of the extracted the 4-bit unsigned divider unit and timing analysis	**10%**
Report	**5%**
Total	**100%**

This project is to be performed in phases and the **deadline** for the various phases is indicated in the table below:

Phase	**Tasks**	**Deadline**
Logic Design & Simulation	1-2	Wednesday, Dec. 12
Transistor-level Design and Spice Analysis	3-5	Wednesday, Jan. 2
Layout Design, Irsim Simulation, and Spice Analysis	6-10	Wednesday, Jan. 16