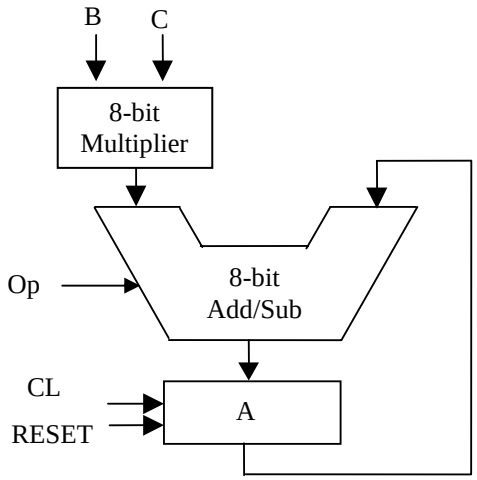
COE 360, Principles of VLSI Design, Term 032
Course Project

Due date: Sunday, May 23

It is required to design an **8-bit Multiply-Accumulate** circuit using CMOS technology. The Multiply-Accumulate circuit shown below is designed using an 8-bit register with a synchronous rising-edge clock, CLK, and **asynchronous** reset, RESET. When RESET=0, the register is reset to 0 asynchronously.



The adder/subtracter used in the design can perform either addition or subtraction. When Op=0, the two operands A and (B*C) are added, i.e. A=A+ (B*C), otherwise they are subtracted i.e. A= A-(B*C). Assume that the numbers are represented in 2's complement notation (except for B and C, assume them unsigned). Design the adder/subtracter circuit to be **modular** i.e. you can easily get an n-bit adder by just duplicating cells. Design your Adder/Subtractor circuit to optimize for **speed**. You need to generate the **carry flag** and the **overflow flag** for your adder/subtracter circuit.

Assume that the multiplier unit is for **unsigned** multiplication. Also, assume that only the least significant 8-bits of the multiplication will be passed to the adder. However, if the result cannot fit in 8-bits i.e. the most significant 8-bits are not equal to 0, then the carry flag should be set to 1 in the current execution cycle. Design your multiplier circuit to be **modular**.

To complete the project, you need to do the following steps for each of the three different components i.e. Adder/Subtractor, Register, Unsigned Multiplier:

1. Assuming a modular design, derive the logic-level implementation of your design.

2. Verify the logic-level design by logic simulation.

3. Derive the transistor-level implementation of your modular cell.

4. Model the transistor-level implementation of your modular cell using SPICE and verify its correct functionality.

5. Determine the worst case propagation delay across your modular cell assuming that all nMOS transistors with a (W/L) ratio of 2, and all pMOS transistors with a (W/L) ratio of 4. For the register, determine the setup and hold time and the FF propagation delay of your design.

6. Draw the stick diagram layout of your modular cell.

7. Using MAGIC, draw the layout of your modular cell assuming that all nMOS transistors are with a (W/L) ratio of 2, and all pMOS transistors are with a (W/L) ratio of 4. Assume that the minimum feature size is used for all transistors.

8. Extract the modular cell of your design from your layout, using the command ***extract***, convert it into the simulator format, using ***ext2sim***, and then simulate it using ***irsim*** and verify that it is working properly for all input combinations.

9. Extract the SPICE model of your modular cell, using the command ***ext2spice***. Then, using SPICE, determine the worst-case transition and propagation delay times of your output signals. Estimate the worst-case propagation delay for the 8-bit circuit of your design.

10. Implement your 8-bit circuit based on the modular cell that you have designed and draw its layout.

11. Extract the 8-bit circuit of your design and verify its correct functionality using irsim.

12. Extract the SPICE model of the 8-bit design and determine the maximum propagation delay across it. Compare this to the estimated worst-case propagation delay obtained in 9. Comment on differences. Determine the maximum frequency under which your design will work properly.

13. Draw the layout of the 8-bit Multiply-Accumulate circuit by connecting the three components together.

14. Verify that the whole design is working properly using ***irsim***. Simulate a 4-bit up/down counter using the designed Multiply-Accumulate.

15. Write a professional report documenting all the design stages of the 8-bit Multiply-Accumulate circuit. All layout plots, circuit diagrams, and SPICE simulation results should be submitted with a final report by the end of the project deadline. Organization and completeness of the report is important.

When extracting your design from Magic, extract it without extracting resistance and capacitances. You can do this by running the following sequence of commands from inside magic:
:Extract no resistance
:Extract no capacitance
:Extract

For SPICE simulation, Use the AMI 0.5U, 5V technology file given in the web link **http://www.ccse.kfupm.edu.sa/~aimane/032/coe360/AMI0.5Uparam.txt**

This project is to be carried out by a team of three students. Each student is supposed to work on one component of the design i.e. register, adder/subtractor, Multiplier. Each student will be evaluated on his component for 90% of the mark. If a team succeeds in having their design work completely, they will get the additional 10%. The distribution of the 90% marks for each student is as follows:

Task	**Mark**
Logic design	**5%**
Verification of logic design by simulation	**5%**
Transistor-level design of the modular cell	**5%**
Spice Simulation of transistor-level design and worst case delay estimation for the modular cell	**10%**
Stick diagram layout of the modular cell	**10%**
Magic layout of the modular cell	**10%**
Logic verification of extracted modular cell using irsim	**5%**
Spice simulation of extracted cell and timing analysis	**10%**
Layout design of 8-bit circuit	**10%**
Logic simulation of 8-bit circuit using irsim	**5%**
Spice simulation of 8-bit circuit and timing analysis	**5%**
Report	**10%**
Total	**90%**