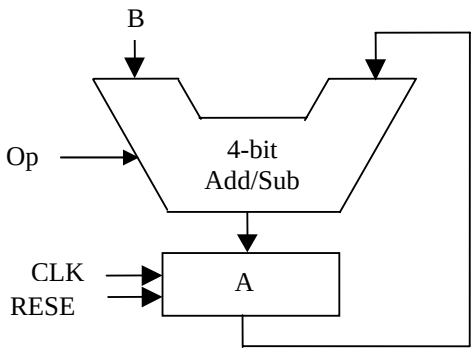
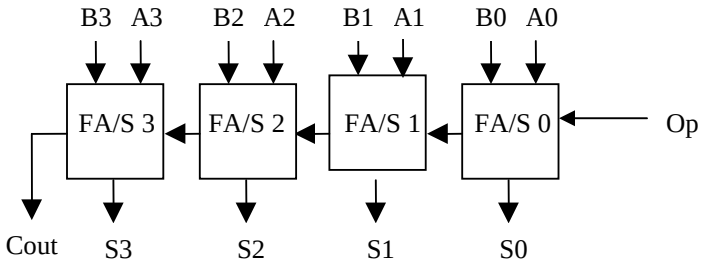
COE 360, Principles of VLSI Design, Term 002
Course Project

Due date: Tuesday, May 29

It is required to design a 4-bit accumulator circuit using CMOS technology. The accumulator circuit shown below is designed using a 4-bit register with a synchronous rising-edge clock, CLK, and asynchronous reset, RESET. When RESET=0, the accumulator is reset to 0 asynchronously.



The adder/subtracter used in the design of the accumulator is a 4-bit ripple-carry adder/subtractor, as shown below. When Op=0, the two operands A and B are added, i.e. A+B, otherwise they are subtracted i.e. A-B. Assume that the numbers are represented in 2's complement notation.



To complete the project, you need to do the following steps:

1. Draw the gate-level schematic of the one-bit full-adder/subtractor circuit.

2. Draw the transistor-level schematic of the one-bit full-adder/subtractor circuit.

3. Draw the stick diagram layout of the one-bit full adder/subtractor circuit.

4. Using MAGIC, draw the layout of the one-bit full adder/subtractor circuit having all nMOS transistors with a (W/L) ratio of 3, and all pMOS transistors with a (W/L) ratio of 6. Assume that the minimum feature size is used for all transistors.

5. Extract the one-bit full-adder/subtractor circuit from your layout, using the command ***extract***, convert it into the simulator format, using ***ext2sim***, and then simulate it using ***irsim*** and verify that it is working properly for all input combinations.

6. Extract the SPICE model of the one-bit full-adder/subtractor circuit, using the command ***ext2spice***. Then, using SPICE, determine the worst-case transition and propagation delay times of the sum and carry-out signals. Estimate the worst-case propagation delay for the 4-bit adder/subtractor.

7. Design your 4-bit adder/subtractor as a cell containing 4 instances of the one-bit full-adder/subtractor cell. Draw the layout of the 4-bit adder/subtractor using the ***array*** command.

8. Connect the 4 full-adder/subtractor cells together to complete the 4-bit adder/subtractor circuit layout. Then, simulate the 4-bit adder/subtractor using ***irsim*** and verify that it is working properly. Verify that it is working properly for the following input combinations for both addition and subtraction:

A	**B**
0000	**0111**
1111	**0111**
0001	**1111**
1111	**1111**
0101	**0101**
0011	**1101**
0111	**0001**
0101	**0011**

9. Extract the SPICE model of the 4-bit adder/subtractor and determine the maximum propagation delay across it. Compare this to the estimated worst-case propagation delay obtained in 6. Comment on differences. Determine the maximum frequency under which the adder/subtractor will work properly.

10. Determine the maximum power dissipated by the 4-bit adder/subtractor using the power meter technique.

11. Draw the transistor-level schematic of the rising-edge triggered DFF with asynchronous set/reset, given in Figure 8.34.

12. Draw the stick diagram layout of the DFF.

13. Draw the layout of the DFF using MAGIC and simulate it using ***irsim*** to verify that it is working properly.

14. Extract the SPICE model of the DFF, and determine the setup time, the hold time and the DFF propagation delay.

15. Construct the layout of a 4-bit register using the DFF layout.

16. Draw the layout of the 4-bit accumulator using the layout of the 4-bit adder and the layout of the 4-bit register.

17. Verify that the whole design is working properly using ***irsim***. Simulate a 4-bit up/down counter using the designed accumulator.

18. Write a professional report documenting all the design stages of the 4-bit accumulator. All layout plots, circuit diagrams, and SPICE simulation results on speed and power should be submitted with a final report by the end of the project deadline. Organization and completeness of the report is important.

This project is to be carried out by a team of three students. The tasks of the project can be divided among the three students as follows:

Student	**Tasks**
1	**1-6, 18**
2	**11-14, 18**
3	**7-10, 15-18**